FIG. 1

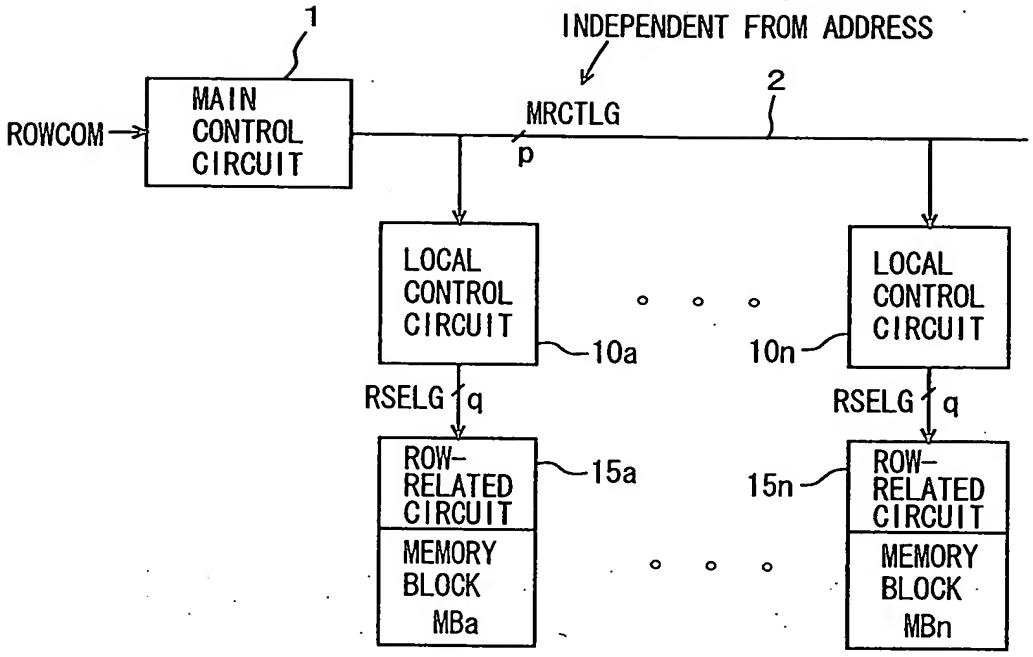

1
INDEPENDENT FROM ADDRESS
ROWCOM
MAIN CONTROL CIRCUIT
MRCTLG
2
p
LOCAL CONTROL CIRCUIT
10a
10n
LOCAL CONTROL CIRCUIT
RSELG
q
RSELG
q
ROW-RELATED CIRCUIT
15a
15n
ROW-RELATED CIRCUIT
MEMORY BLOCK
MBa
MEMORY BLOCK
MBn

FIG. 2

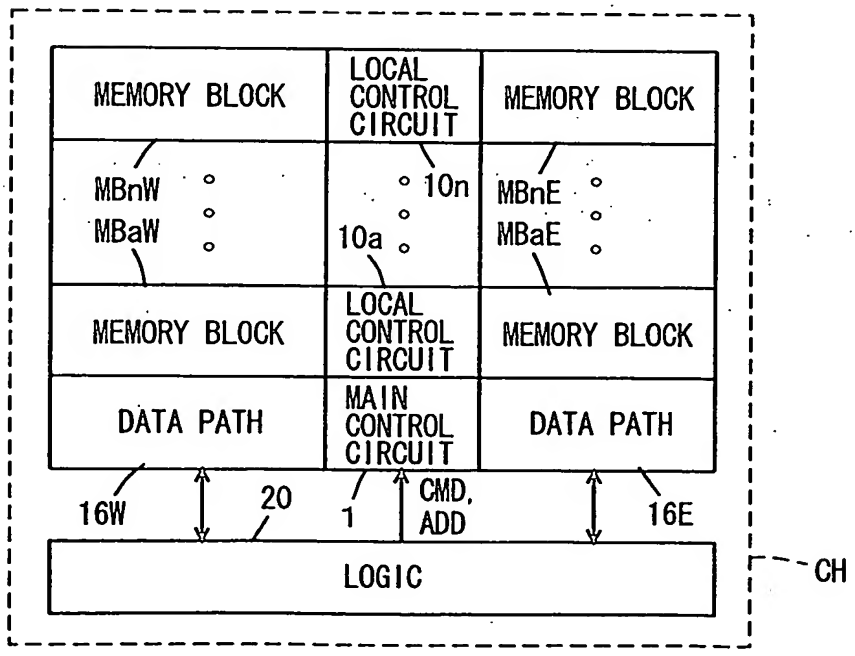

MEMORY BLOCK
LOCAL CONTROL CIRCUIT
MEMORY BLOCK
MBnW
MBaW
10n
10a
MBnE
MBaE
MEMORY BLOCK
LOCAL CONTROL CIRCUIT
MEMORY BLOCK
DATA PATH
MAIN CONTROL CIRCUIT
DATA PATH
16W
20
1
CMD, ADD
16E
LOGIC
CH

FIG. 3

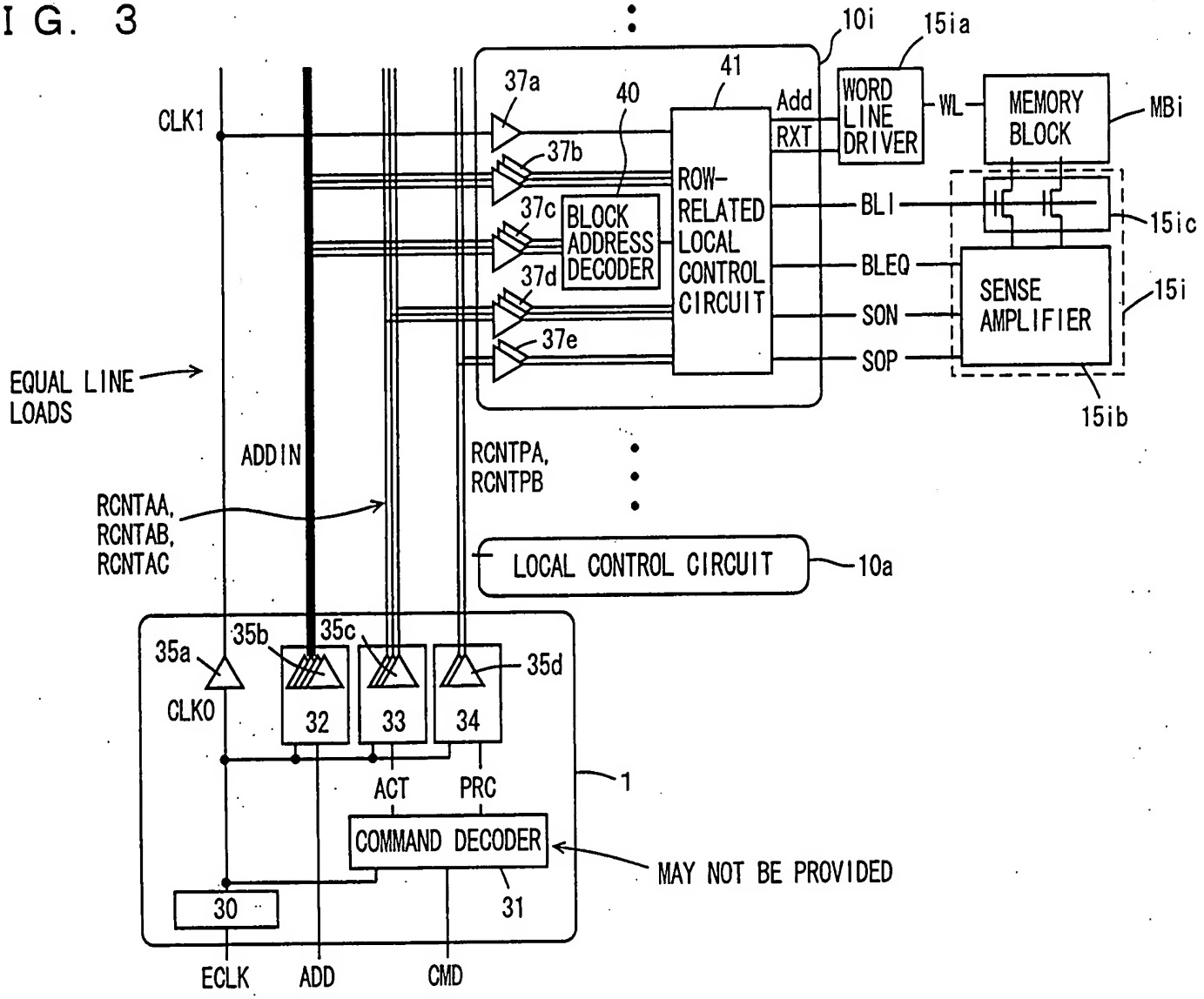

10i
15ia
41
37a
40
Add
WORD LINE DRIVER
WL
MEMORY BLOCK
MBi
CLK1
37b
RXT
37c
BLOCK ADDRESS DECODER
ROW-RELATED LOCAL CONTROL CIRCUIT
BLI
15ic
37d
BLEQ
SENSE AMPLIFIER
15i
37e
SON
SOP
EQUAL LINE LOADS
15ib
ADDIN
RCNTPA, RCNTPB
RCNTAA, RCNTAB, RCNTAC
LOCAL CONTROL CIRCUIT
10a
35a
35b
35c
35d
CLKO
32
33
34
ACT
PRC
1
COMMAND DECODER
MAY NOT BE PROVIDED
30
31
ECLK
ADD
CMD

FIG. 4

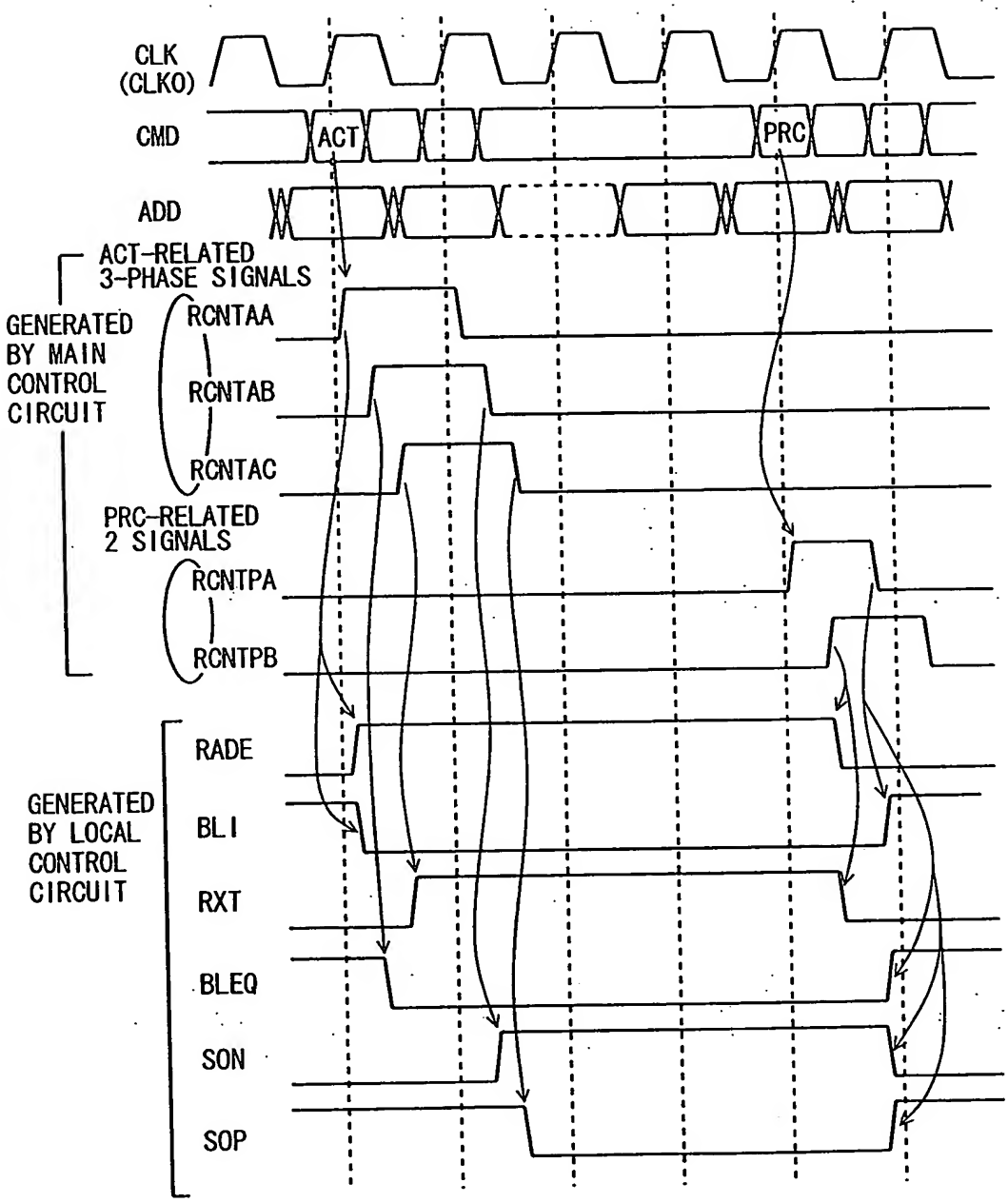

CLK
(CLKO)
CMD
ACT
PRC
ADD
ACT-RELATED
3-PHASE SIGNALS
GENERATED
BY MAIN
CONTROL
CIRCUIT
RCNTAA
RCNTAB
RCNTAC
PRC-RELATED
2 SIGNALS
RCNTPA
RCNTPB
GENERATED
BY LOCAL
CONTROL
CIRCUIT
RADE
BLI
RXT
BLEQ
SON
SOP

FIG. 5

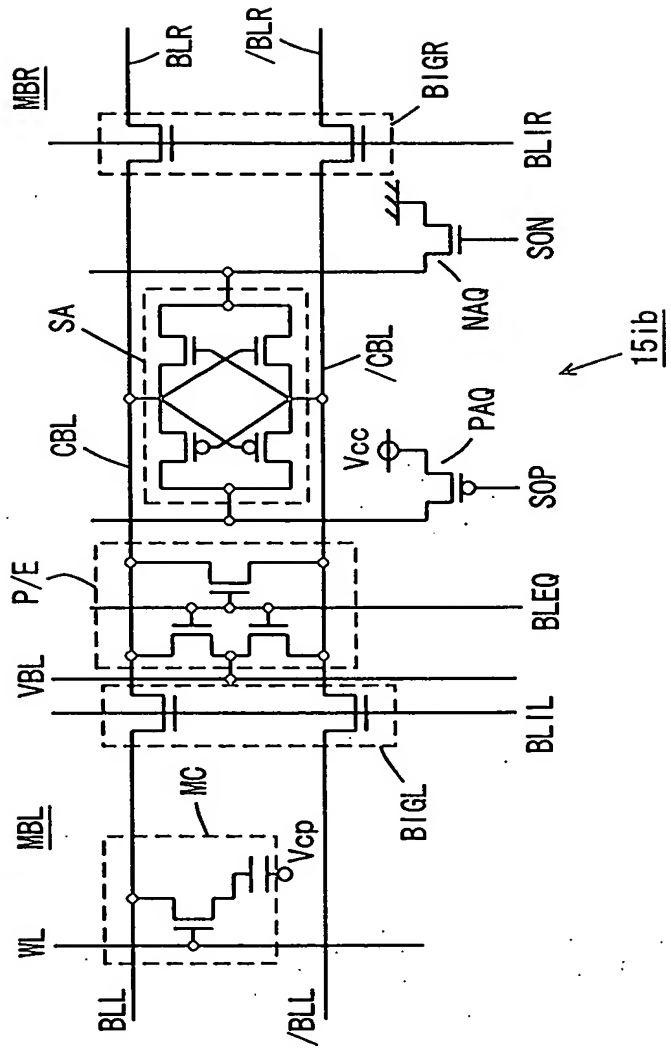

MBR
BLR
/BLR
BIGR
BLIR
SON
NAQ
SA
/CBL
CBL
Vcc
PAQ
SOP
15ib
P/E
BLEQ
VBL
BLIL
MBL
MC
Vcp
BIGL
WL
BLL
/BLL

FIG. 6

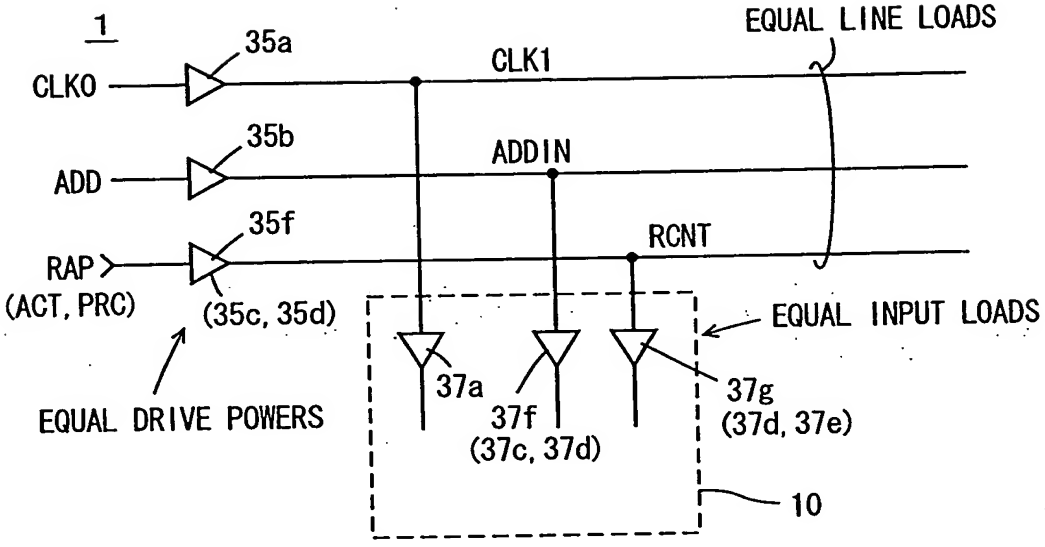

1
35a
CLK0
CLK1
EQUAL LINE LOADS
35b
ADD
ADDIN
35f
RAP
(ACT, PRC)
(35c, 35d)
RCNT
EQUAL INPUT LOADS
EQUAL DRIVE POWERS
37a
37f
(37c, 37d)
37g
(37d, 37e)
10

FIG. 7

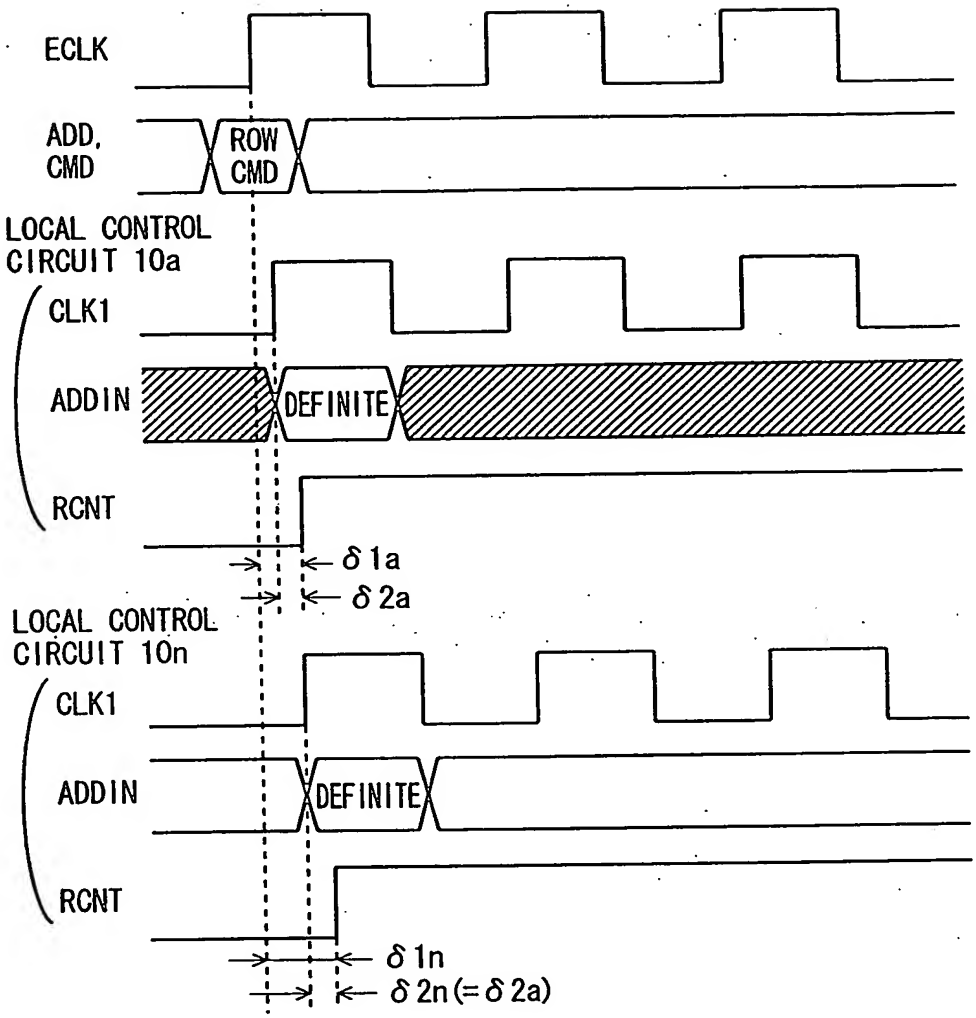

ECLK
ADD, CMD
ROW CMD
LOCAL CONTROL CIRCUIT 10a
CLK1
ADDIN
DEFINITE
RCNT
δ 1a
δ 2a
LOCAL CONTROL CIRCUIT 10n
CLK1
ADDIN
DEFINITE
RCNT
δ 1n
δ 2n (= δ 2a)

FIG. 8

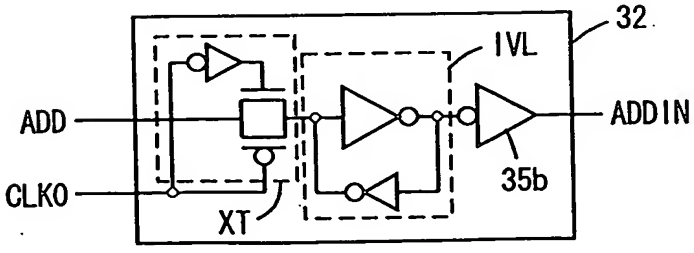

32
IVL
ADD
ADDIN
CLKO
35b
XT

FIG. 9A

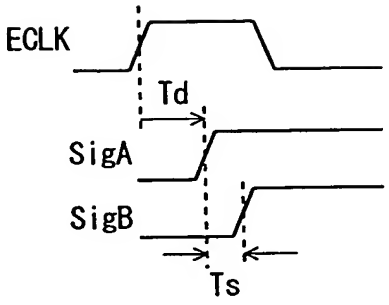



FIG. 9B PRIOR ART

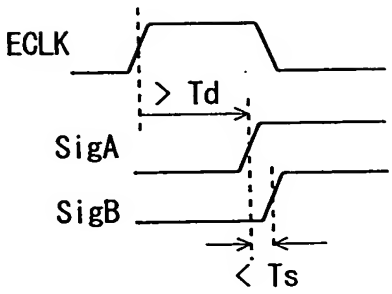



FIG. 9C

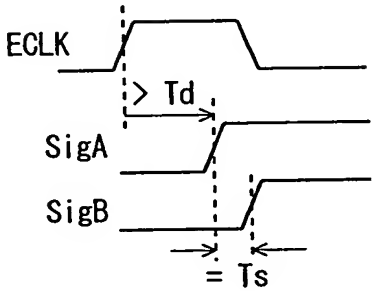


FIG. 10A

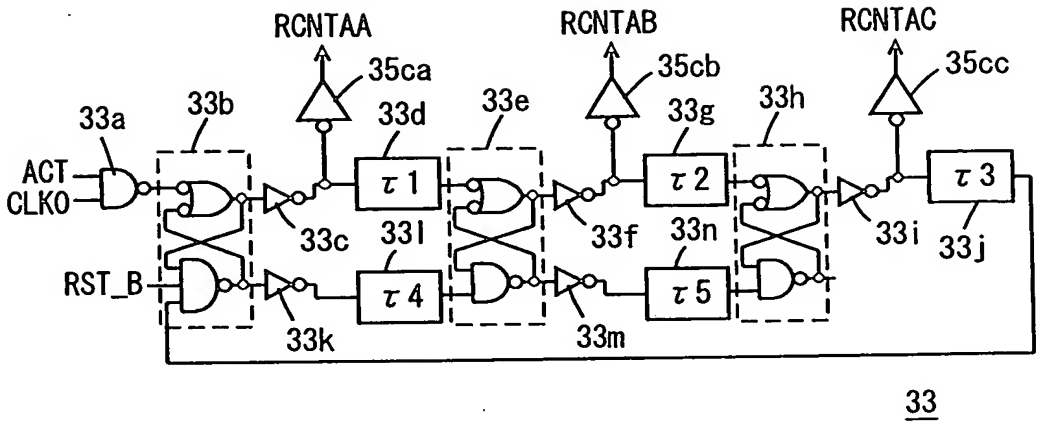



FIG. 10B

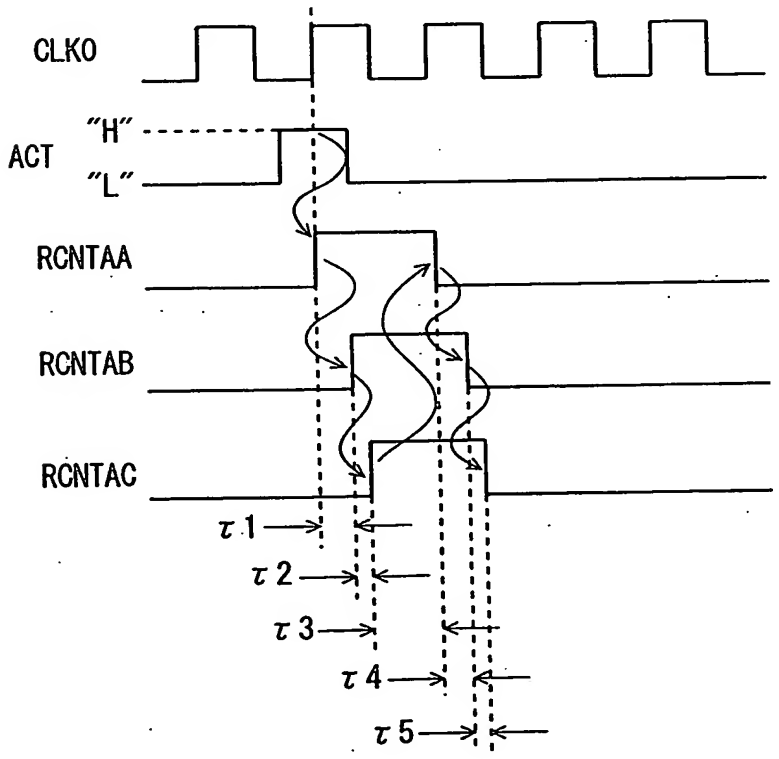


FIG. 11A

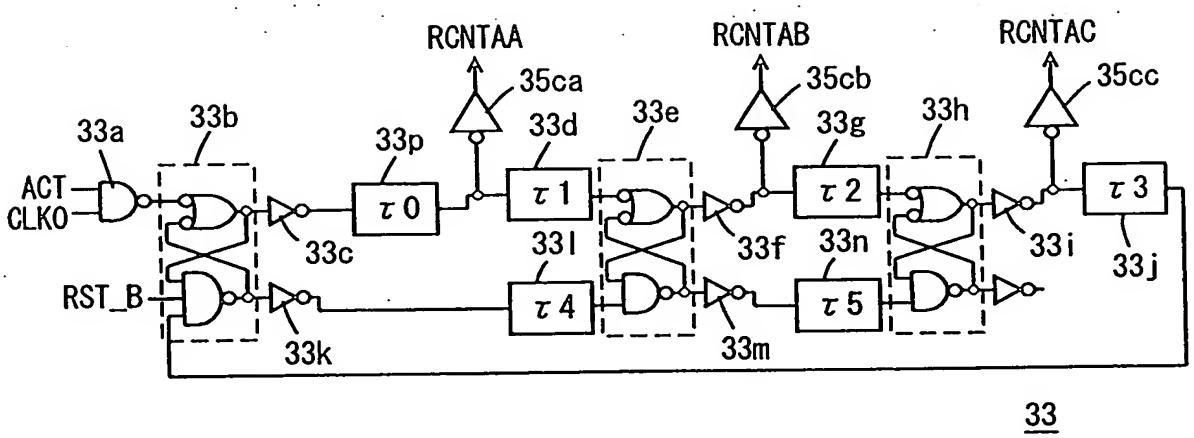



FIG. 11B

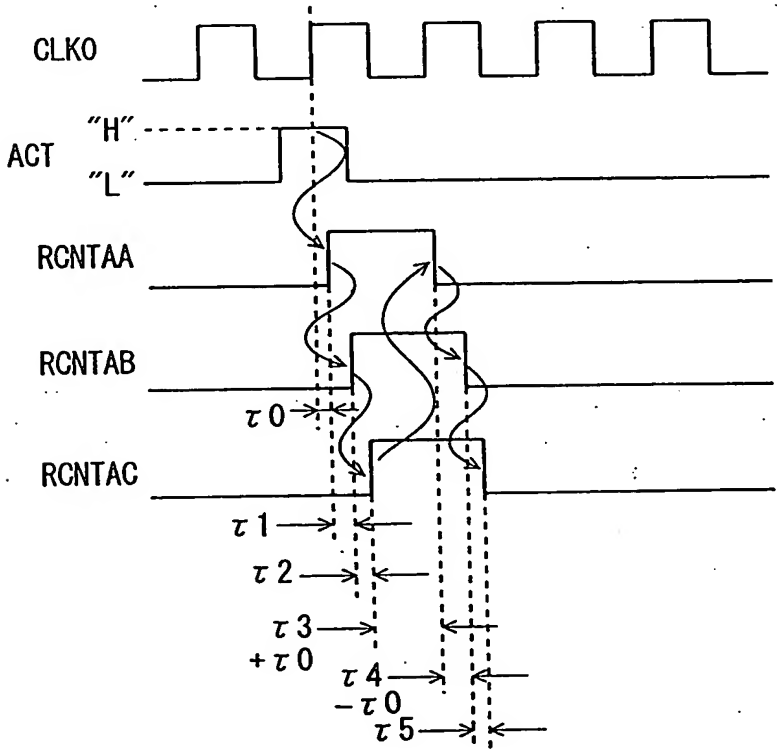


FIG. 12A

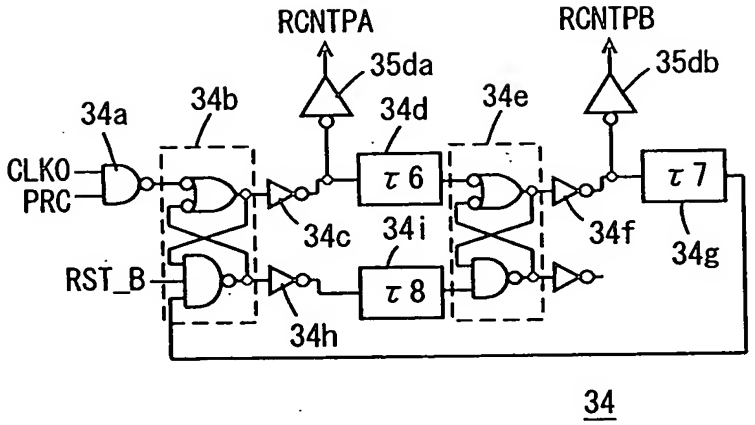



FIG. 12B

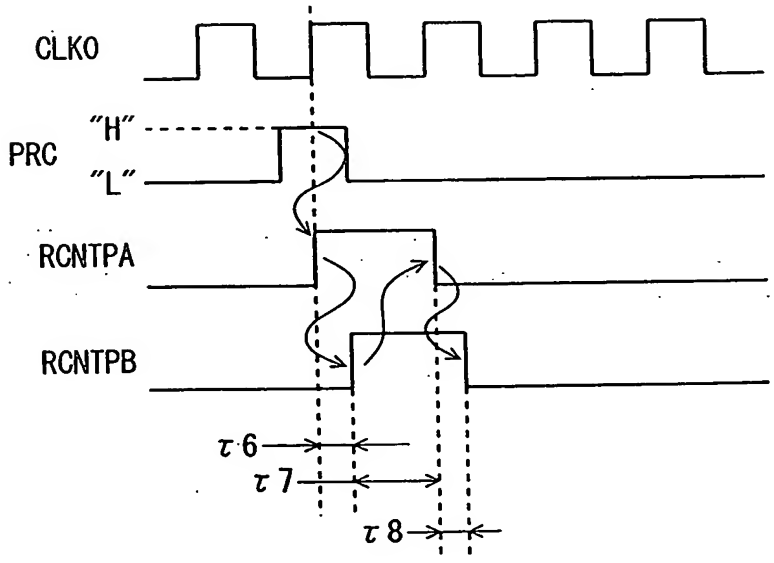


FIG. 13A

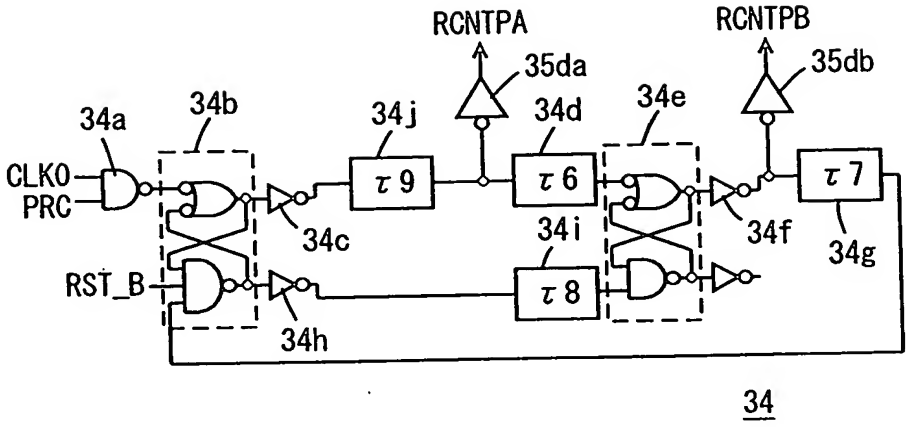



FIG. 13B

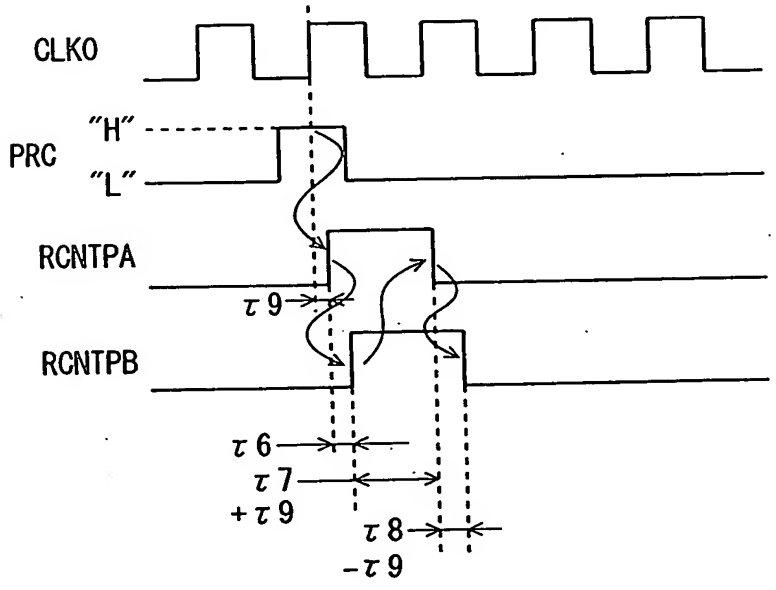


FIG. 14

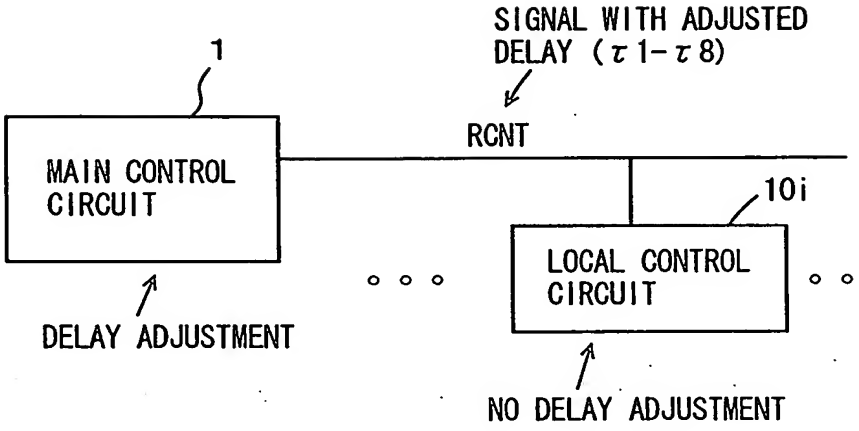

SIGNAL WITH ADJUSTED DELAY (τ1-τ8)
1
RCNT
MAIN CONTROL CIRCUIT
10i
LOCAL CONTROL CIRCUIT
DELAY ADJUSTMENT
NO DELAY ADJUSTMENT

FIG. 15A

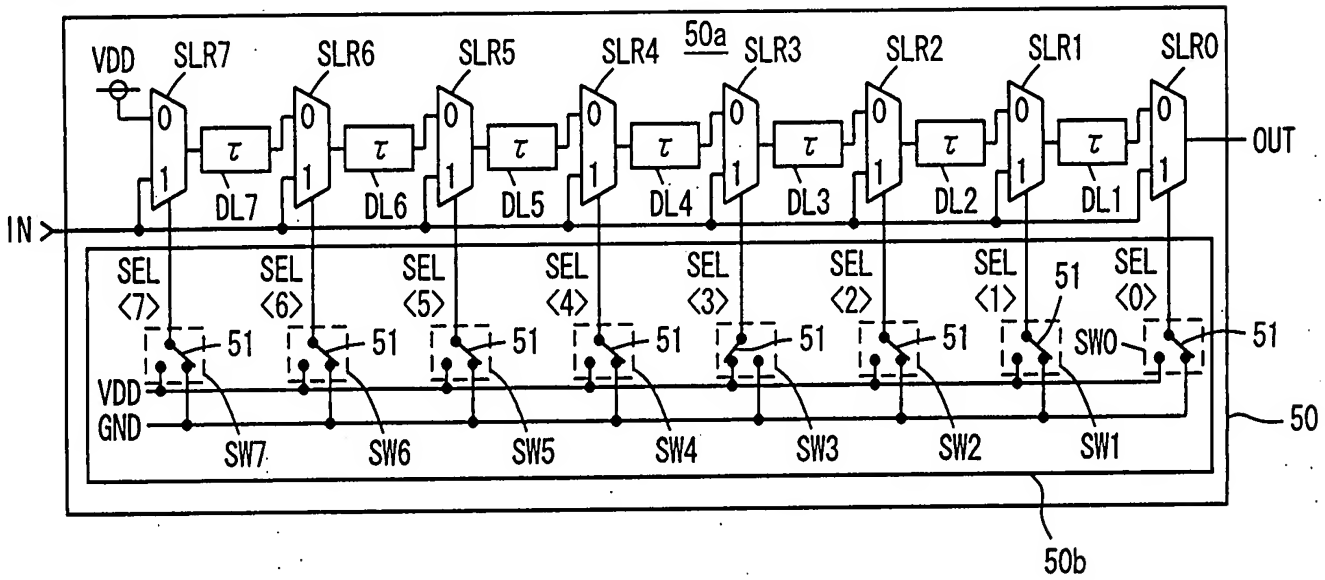



FIG. 15B

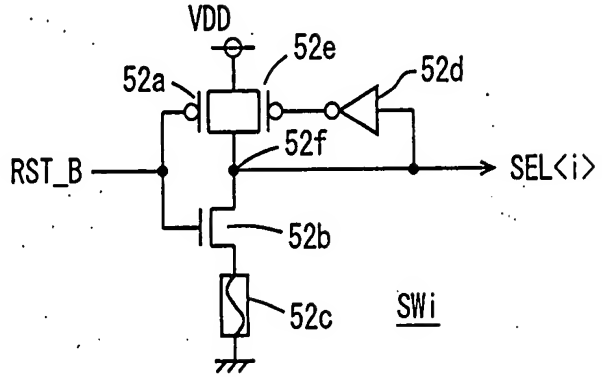


FIG. 16

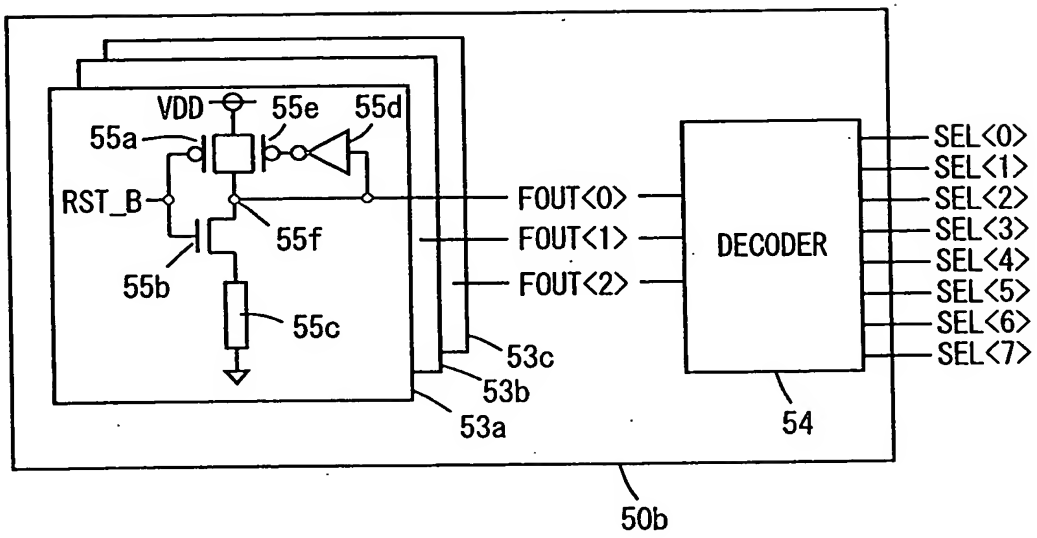

VDD
55e
55d
55a
RST_B
55f
55b
55c
FOUT<0>
FOUT<1>
FOUT<2>
DECODER
SEL<0>
SEL<1>
SEL<2>
SEL<3>
SEL<4>
SEL<5>
SEL<6>
SEL<7>
53c
53b
53a
54
50b

FIG. 17

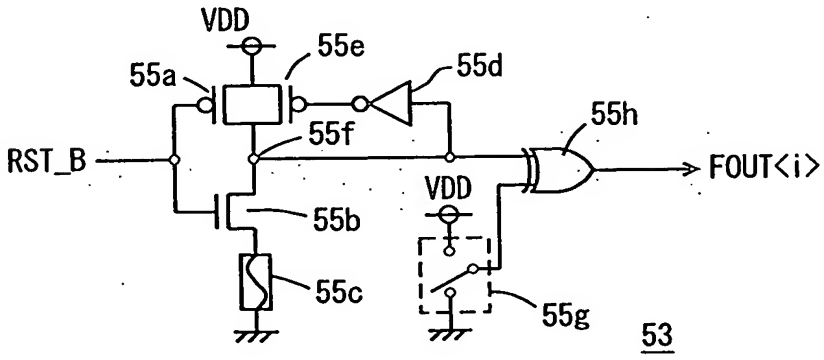

VDD
55e
55a
55d
55h
55f
RST_B
FOUT<i>
VDD
55b
55c
55g
53

FIG. 18

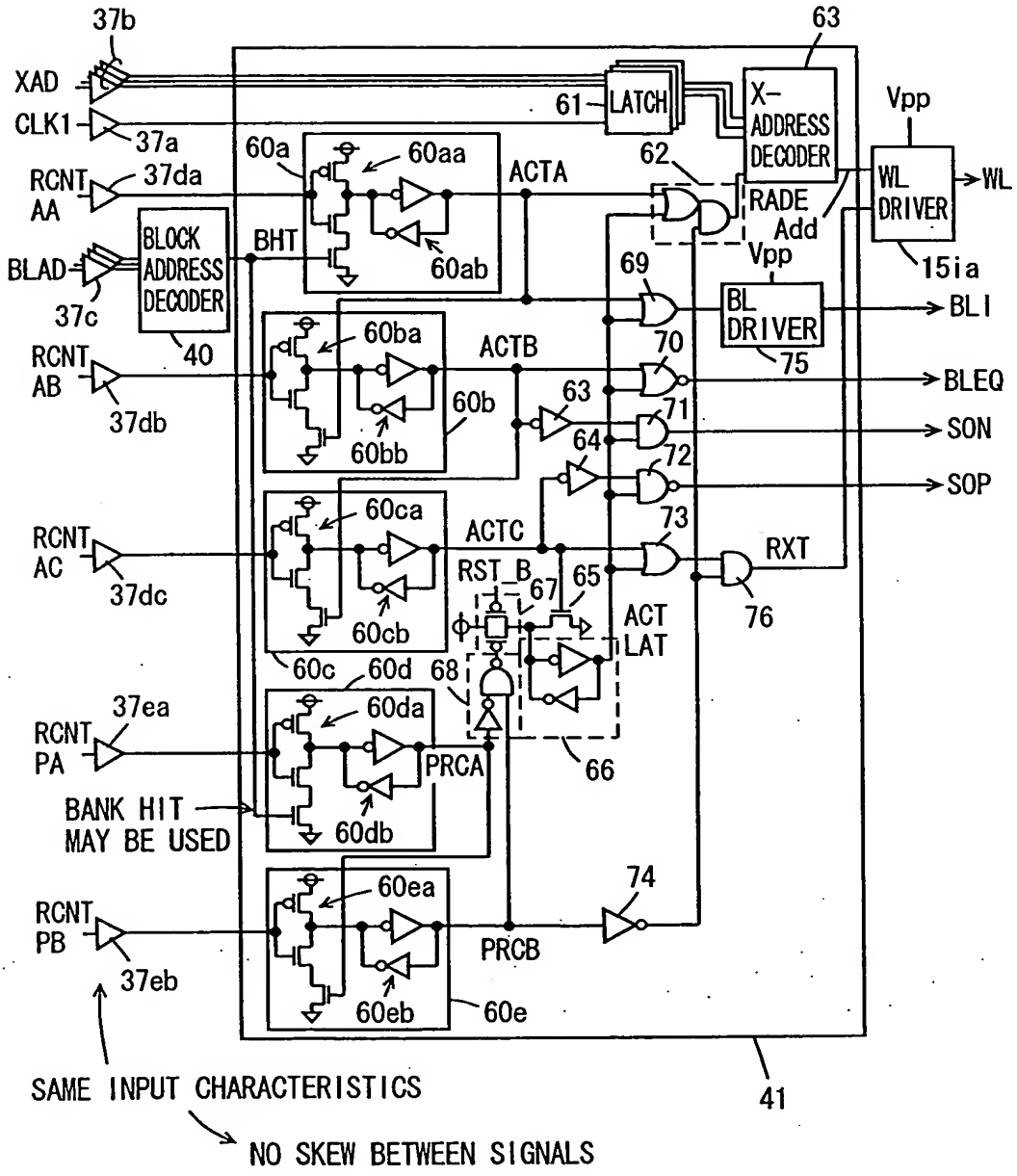

37b
XAD
CLK1
37a
RCNT AA
37da
BLAD
37c
BLOCK ADDRESS DECODER
40
BHT
60a
60aa
60ab
ACTA
61
LATCH
63
X-ADDRESS DECODER
62
RADE
Add
Vpp
WL DRIVER
WL
15ia
Vpp
69
BL DRIVER
75
BLI
RCNT AB
37db
60ba
60bb
60b
ACTB
70
BLEQ
63
71
SON
64
72
SOP
RCNT AC
37dc
60ca
60cb
60c
ACTC
73
RXT
RST_B
67
65
76
ACT LAT
60d
68
66
37ea
RCNT PA
60da
60db
PRCA
BANK HIT MAY BE USED
74
RCNT PB
37eb
60ea
60eb
60e
PRCB
SAME INPUT CHARACTERISTICS
NO SKEW BETWEEN SIGNALS
41

FIG. 19

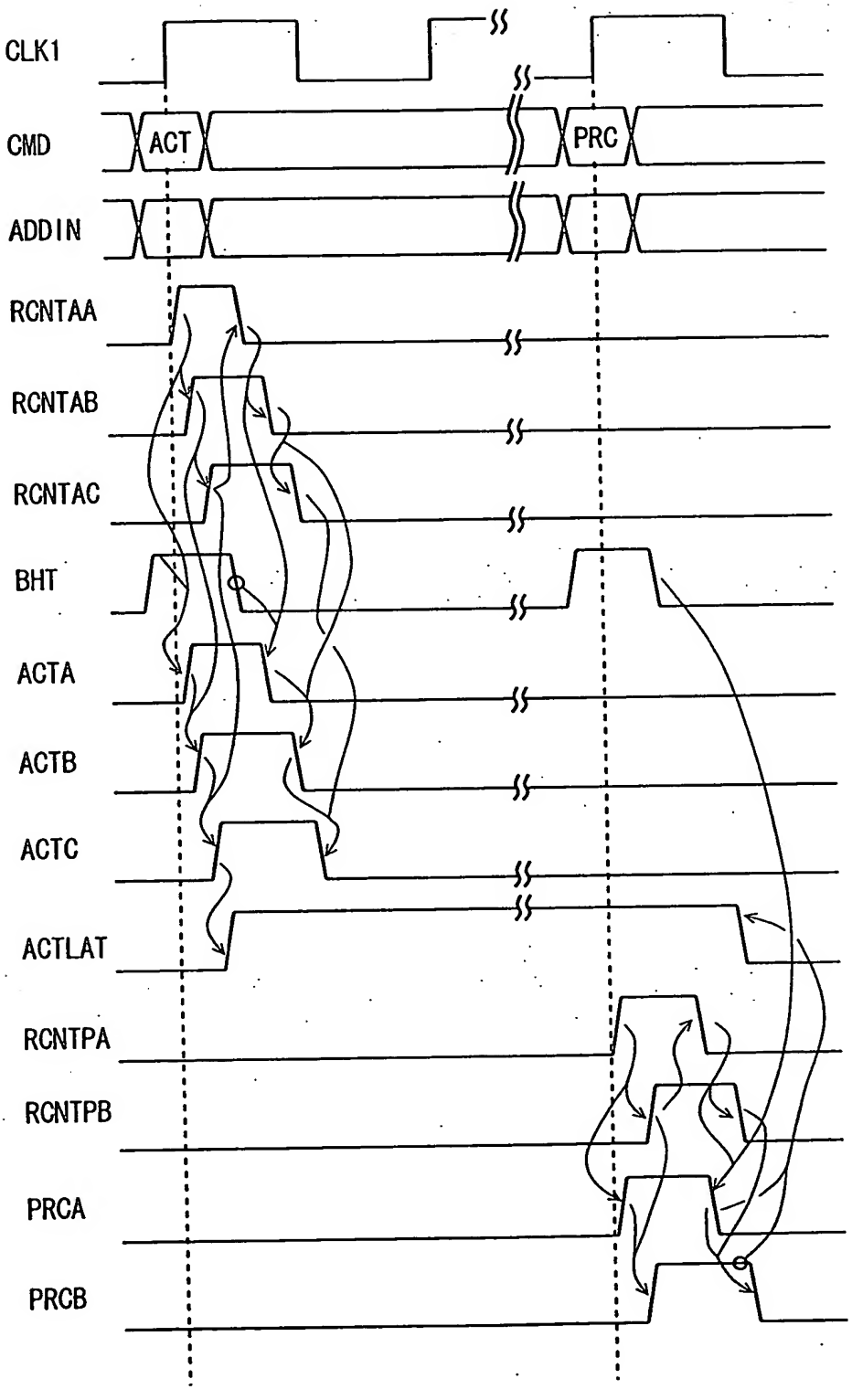

CLK1
CMD
ACT
PRC
ADDIN
RCNTAA
RCNTAB
RCNTAC
BHT
ACTA
ACTB
ACTC
ACTLAT
RCNTPA
RCNTPB
PRCA
PRCB

FIG. 20

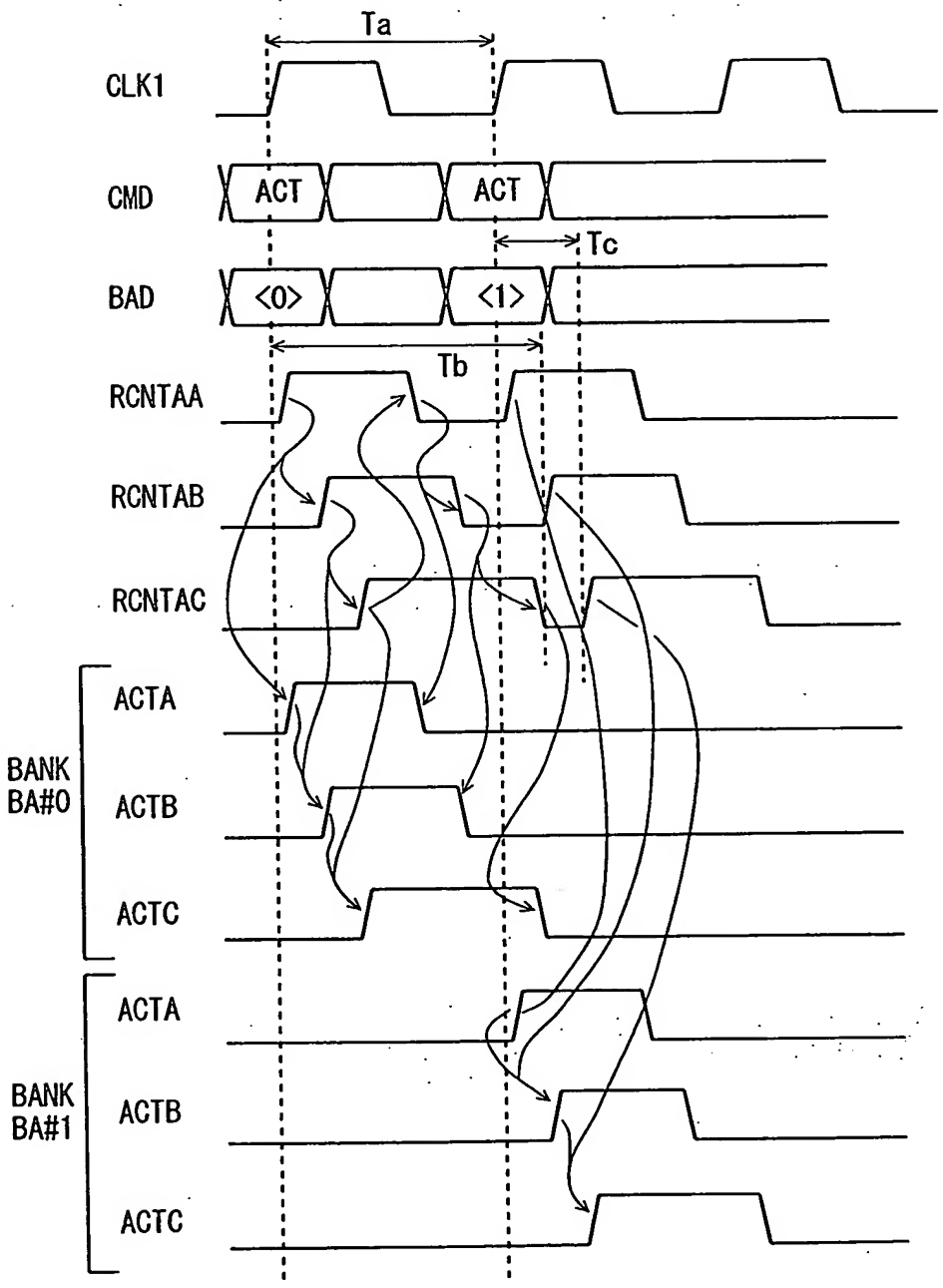

Ta
CLK1
CMD
ACT
ACT
Tc
BAD
<0>
<1>
Tb
RCNTAA
RCNTAB
RCNTAC
BANK BA#0
ACTA
ACTB
ACTC
BANK BA#1
ACTA
ACTB
ACTC

FIG. 21

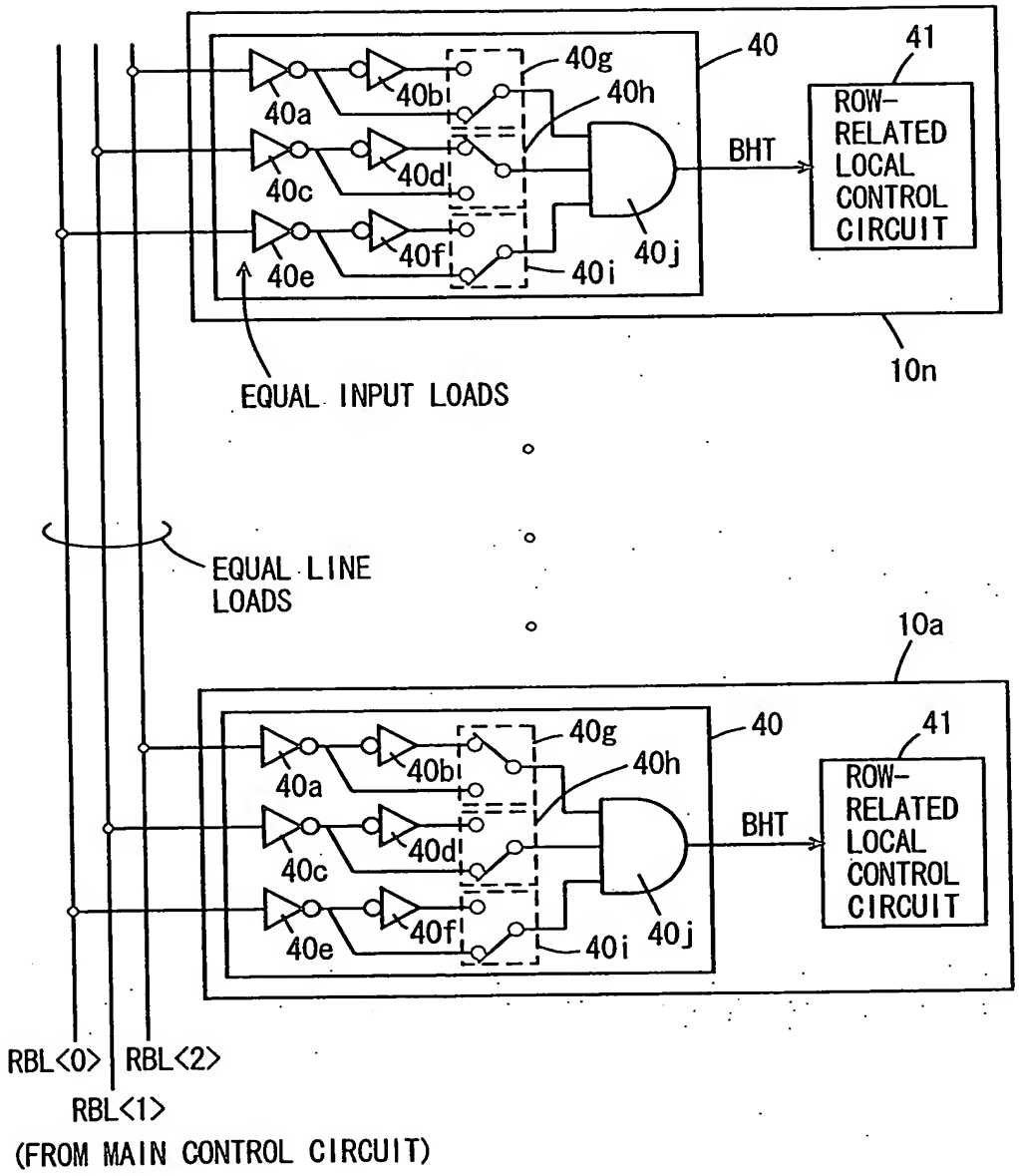

40
41
40g
40h
40a
40b
40c
40d
40e
40f
40i
40j
BHT
ROW-
RELATED
LOCAL
CONTROL
CIRCUIT
10n
EQUAL INPUT LOADS
EQUAL LINE
LOADS
10a
RBL<0>
RBL<2>
RBL<1>
(FROM MAIN CONTROL CIRCUIT)

FIG. 22

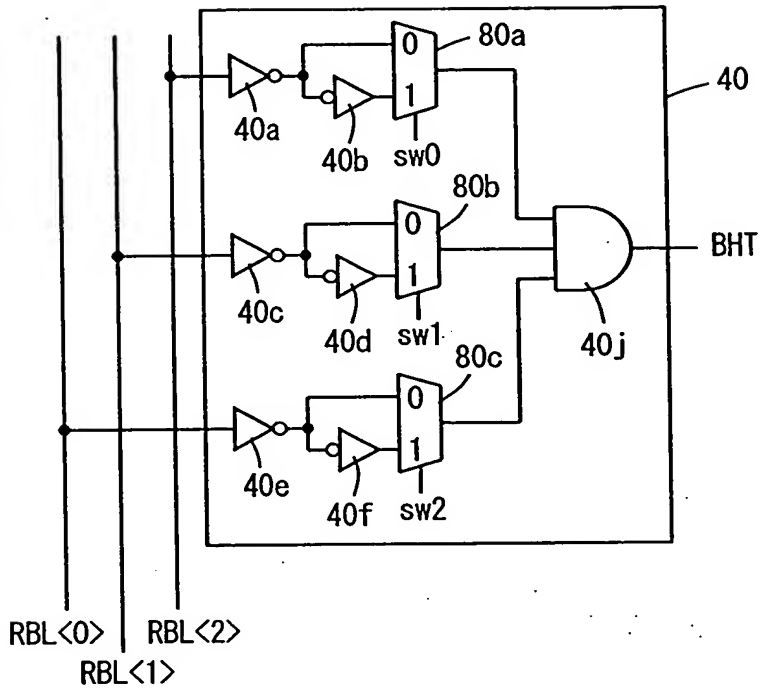

80a
40
40a
40b
sw0
80b
BHT
40c
40d
sw1
40j
80c
40e
40f
sw2
RBL<0>
RBL<2>
RBL<1>

FIG. 23

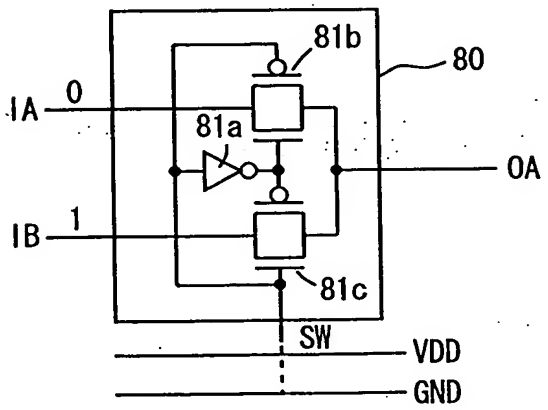

81b
80
IA
0
81a
OA
IB
1
81c
SW
VDD
GND

FIG. 24

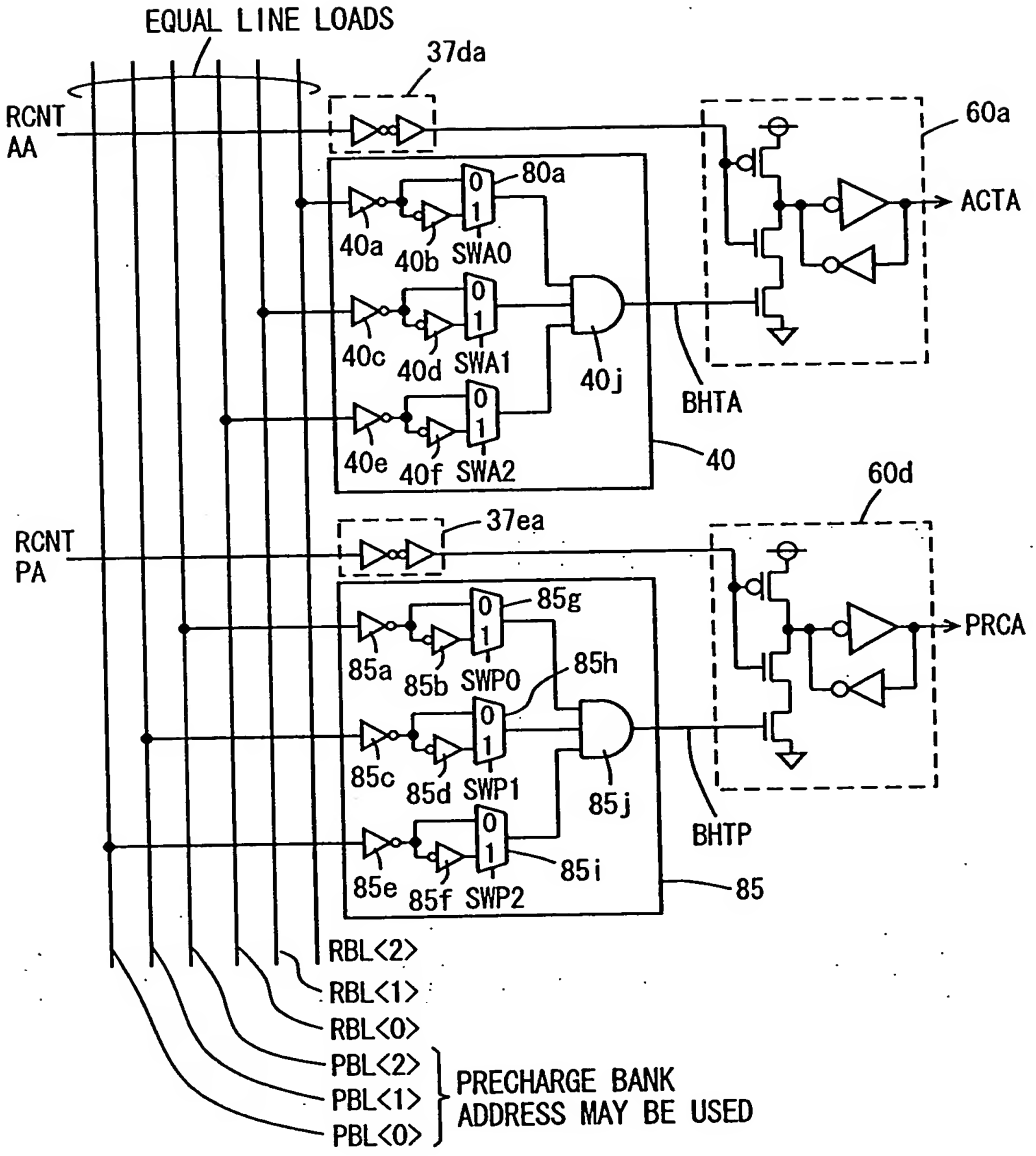
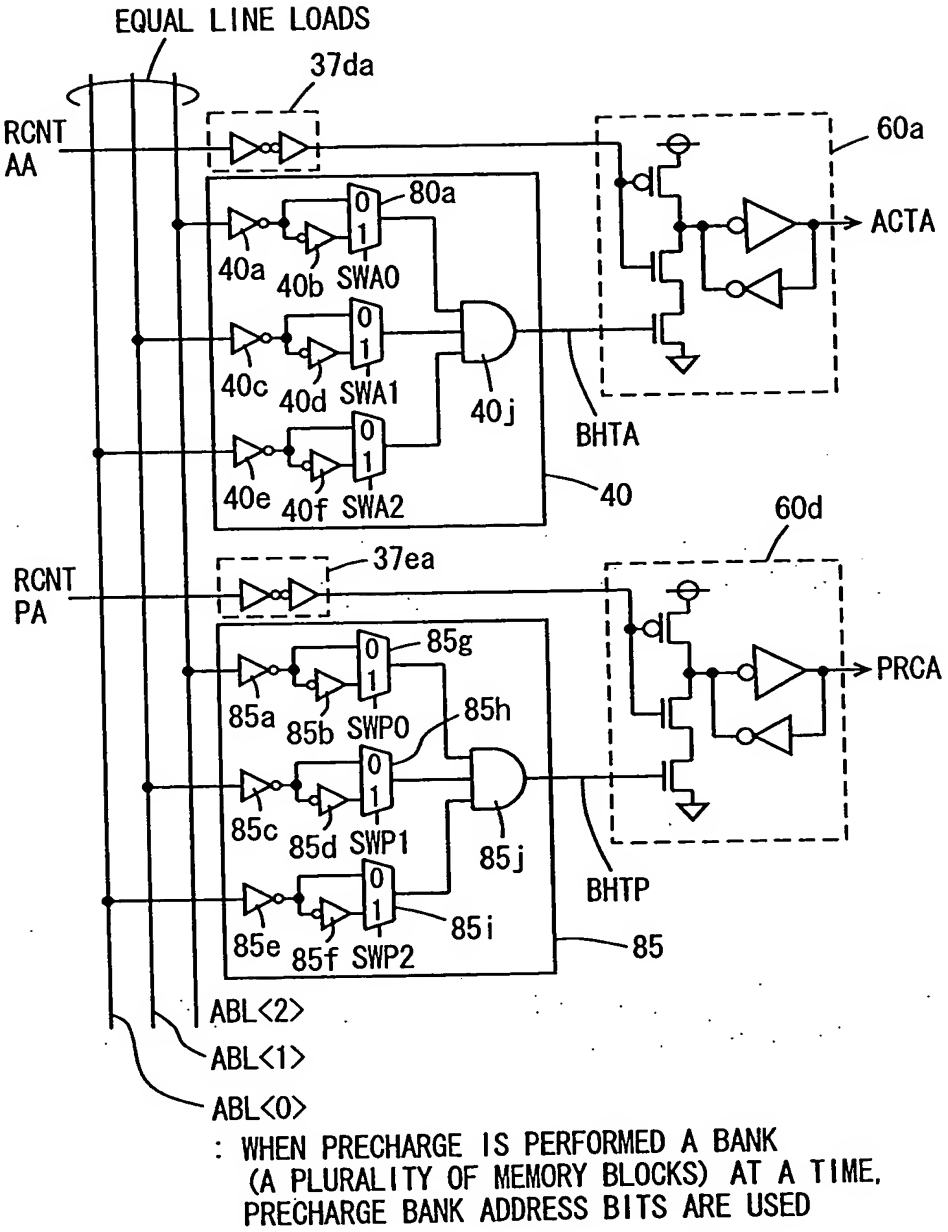

EQUAL LINE LOADS
37da
RCNT
AA
60a
80a
ACTA
40a
40b
SWA0
40c
40d
SWA1
40j
BHTA
40e
40f
SWA2
40
60d
37ea
RCNT
PA
85g
PRCA
85a
85b
SWP0
85h
85c
85d
SWP1
85j
BHTP
85e
85f
SWP2
85i
85
RBL<2>
RBL<1>
RBL<0>
PBL<2>
PBL<1>
PBL<0>
PRECHARGE BANK
ADDRESS MAY BE USED

FIG. 25




: WHEN PRECHARGE IS PERFORMED A BANK (A PLURALITY OF MEMORY BLOCKS) AT A TIME, PRECHARGE BANK ADDRESS BITS ARE USED

FIG. 26

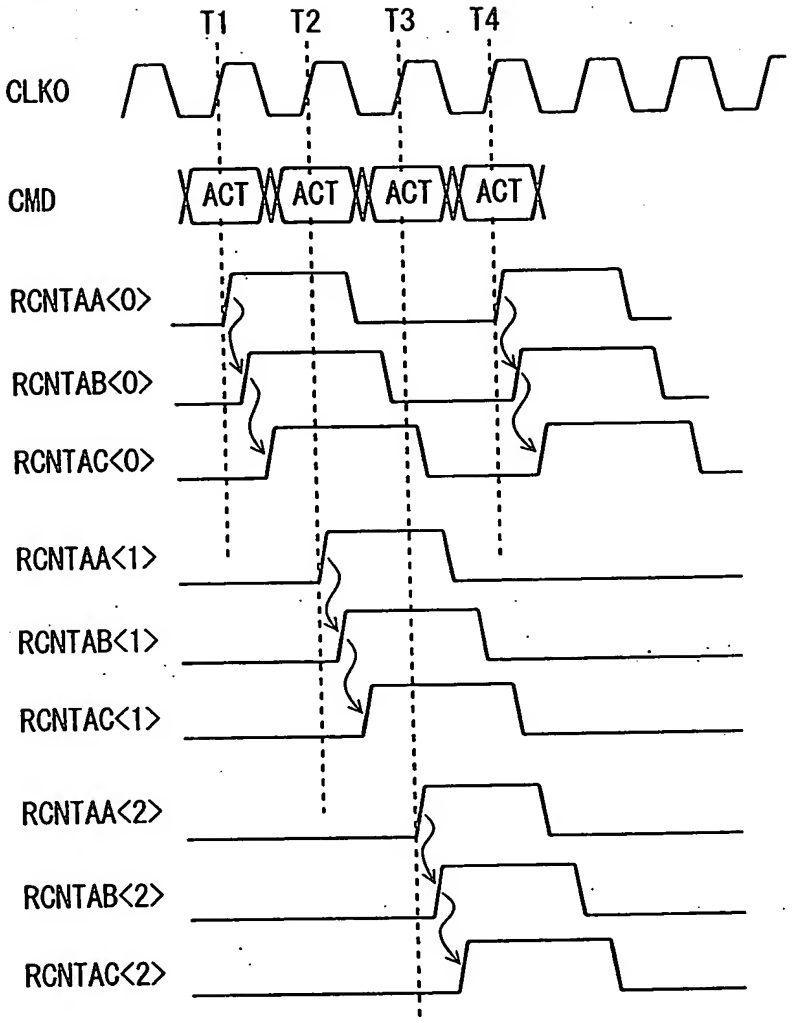

T1
T2
T3
T4
CLKO
CMD
ACT
ACT
ACT
ACT
RCNTAA<0>
RCNTAB<0>
RCNTAC<0>
RCNTAA<1>
RCNTAB<1>
RCNTAC<1>
RCNTAA<2>
RCNTAB<2>
RCNTAC<2>

FIG. 27

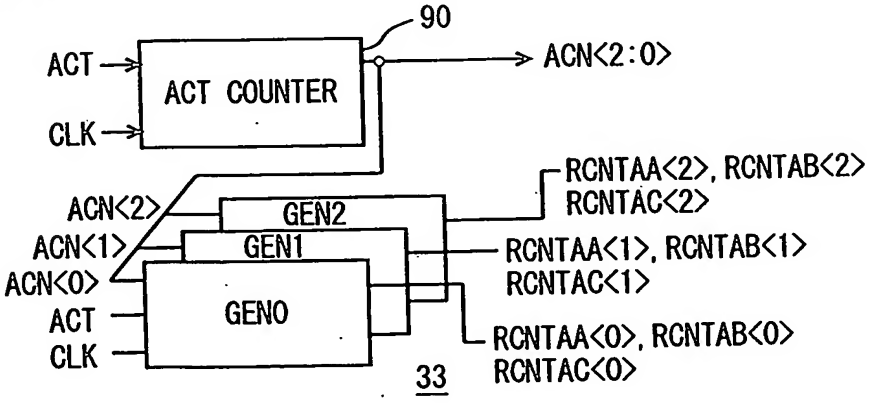

90
ACT
CLK
ACT COUNTER
ACN<2:0>
ACN<2>
ACN<1>
ACN<0>
GEN2
GEN1
GEN0
ACT
CLK
RCNTAA<2>, RCNTAB<2>
RCNTAC<2>
RCNTAA<1>, RCNTAB<1>
RCNTAC<1>
RCNTAA<0>, RCNTAB<0>
RCNTAC<0>
33

FIG. 28A

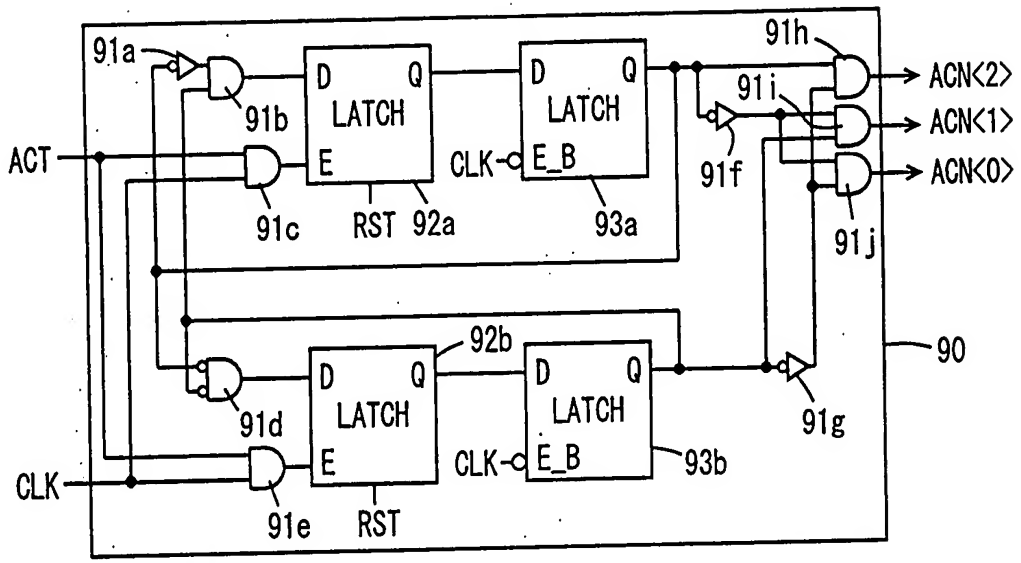



FIG. 28B

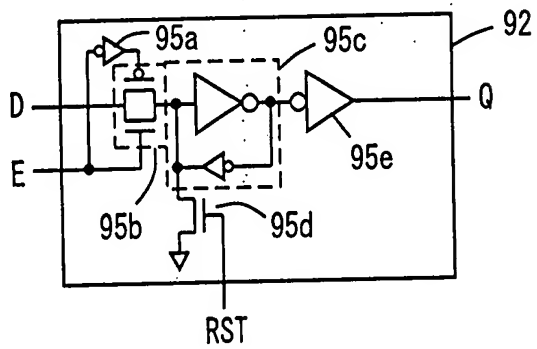



FIG. 28C

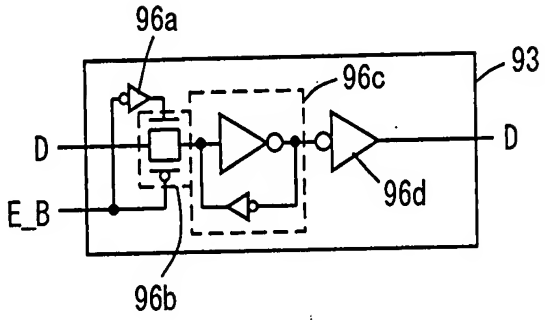


FIG. 29

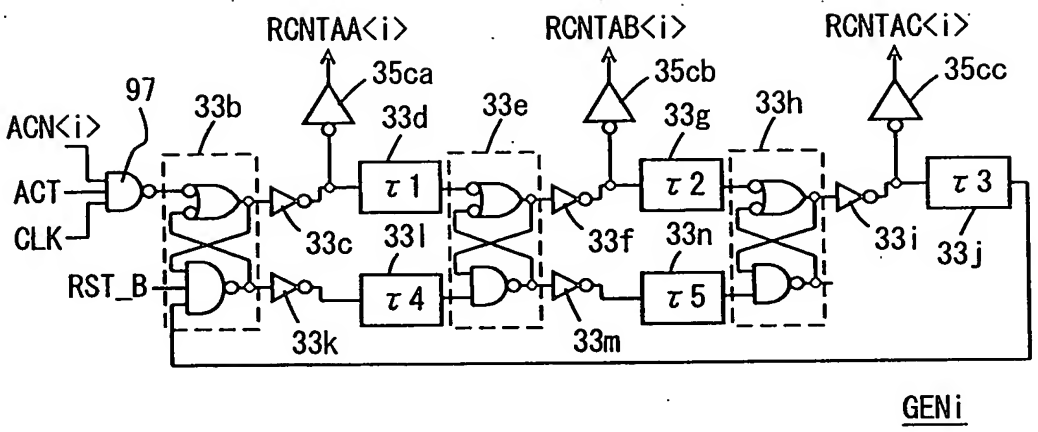



FIG. 30

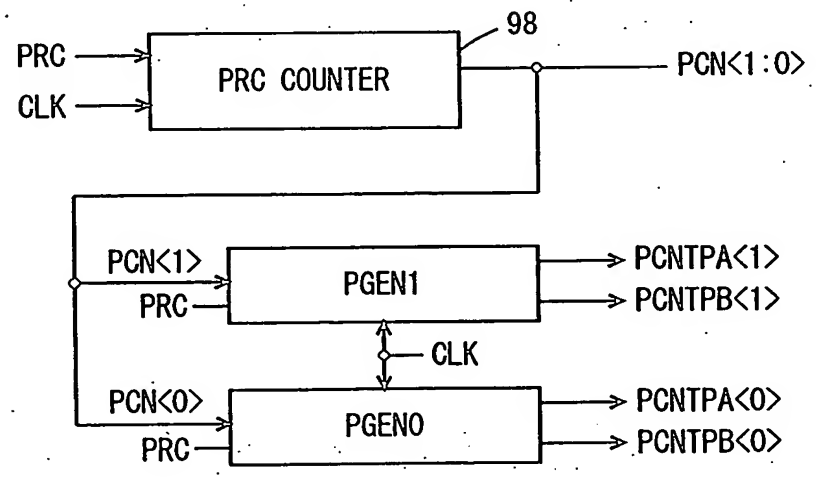



FIG. 31

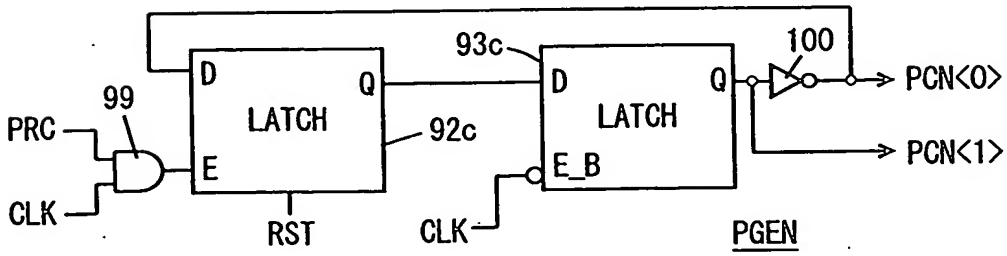


FIG. 32

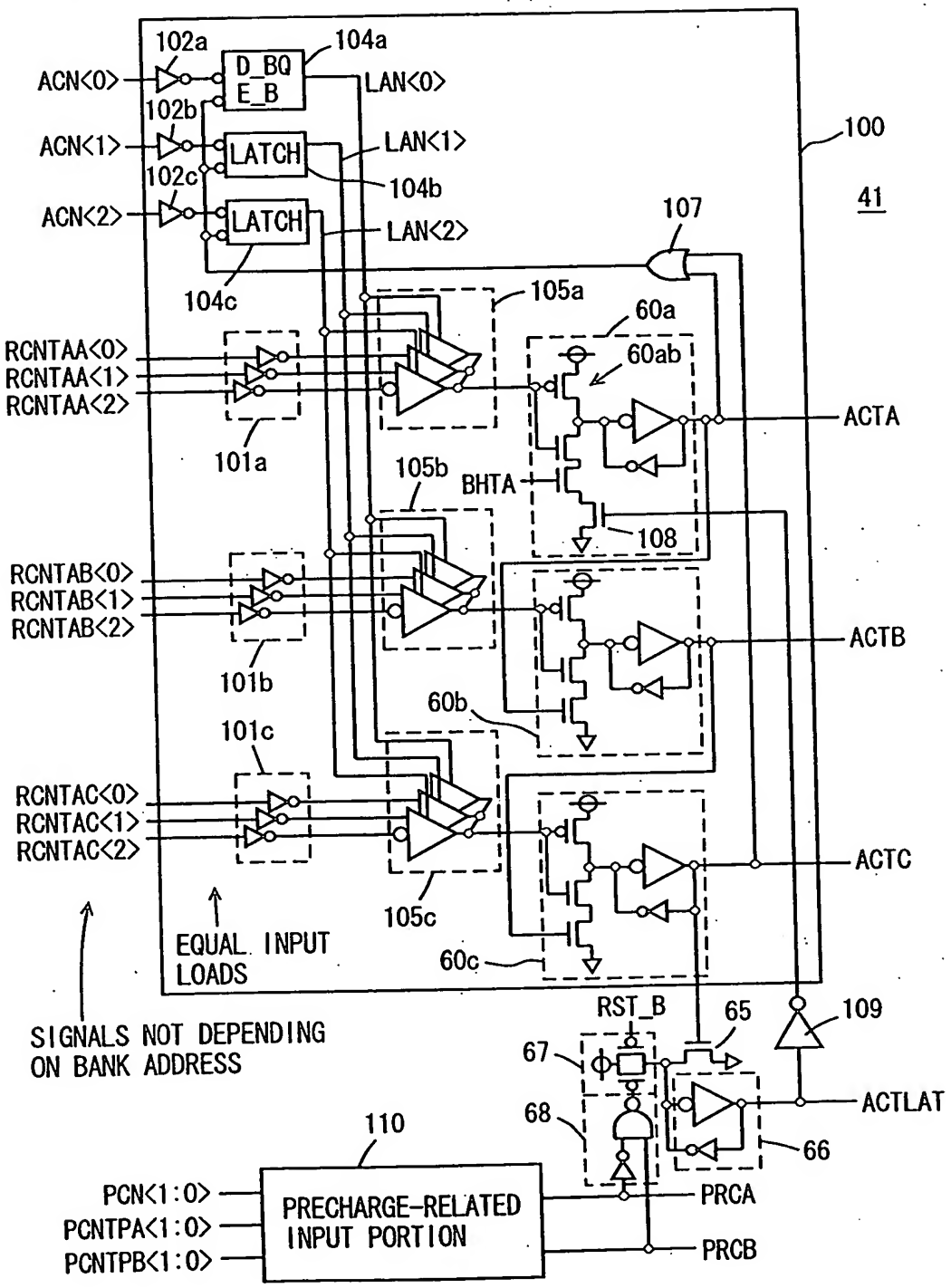

ACN<0>
ACN<1>
ACN<2>
102a
102b
102c
D_BQ
E_B
LATCH
LATCH
104a
104b
104c
LAN<0>
LAN<1>
LAN<2>
100
41
107
105a
60a
60ab
RCNTAA<0>
RCNTAA<1>
RCNTAA<2>
101a
ACTA
105b
BHTA
108
RCNTAB<0>
RCNTAB<1>
RCNTAB<2>
101b
ACTB
60b
101c
RCNTAC<0>
RCNTAC<1>
RCNTAC<2>
ACTC
105c
EQUAL INPUT LOADS
60c
SIGNALS NOT DEPENDING ON BANK ADDRESS
RST_B
65
109
67
ACTLAT
68
66
110
PCN<1:0>
PCNTPA<1:0>
PCNTPB<1:0>
PRECHARGE-RELATED INPUT PORTION
PRCA
PRCB

FIG. 33

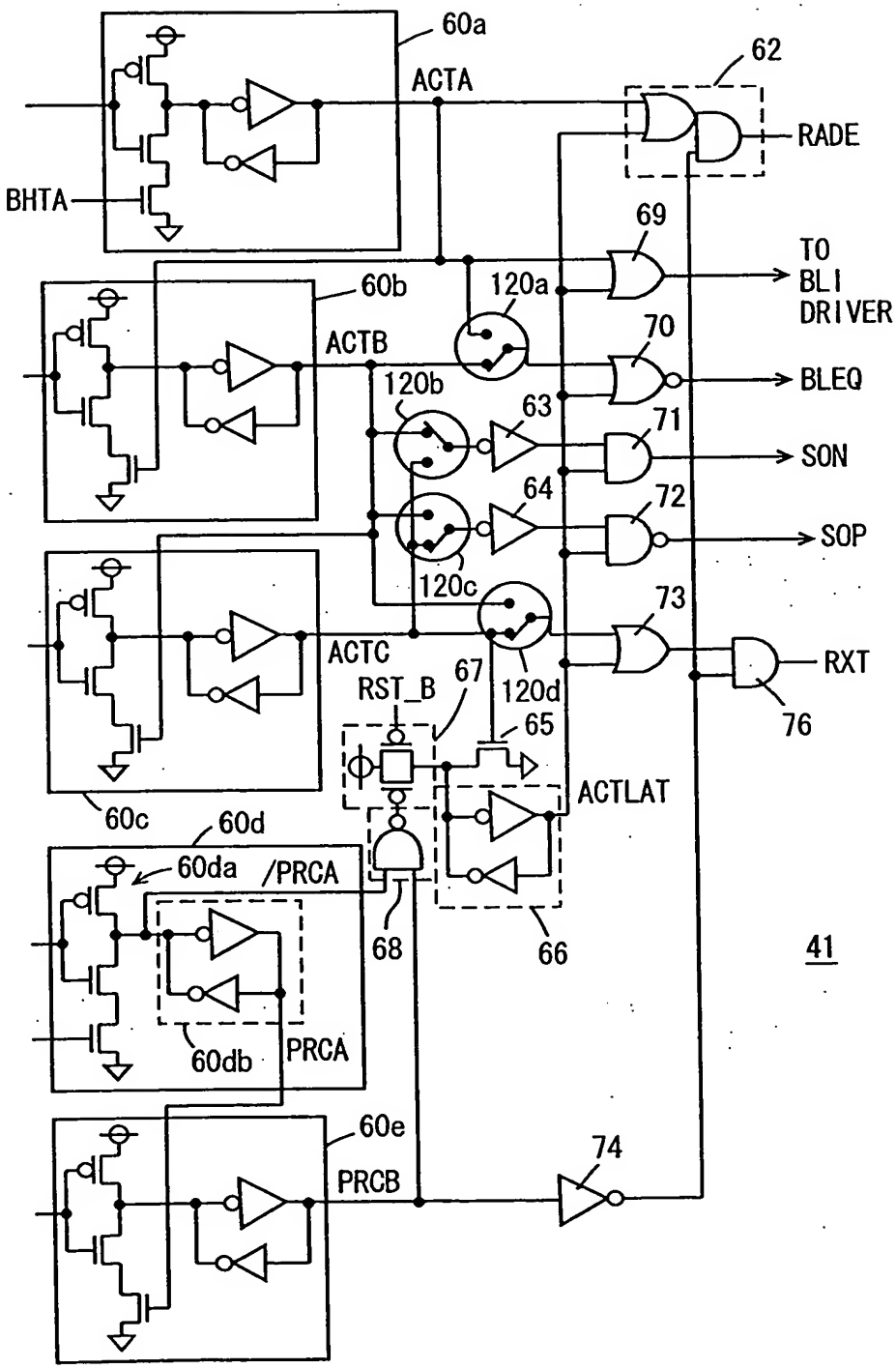

60a
ACTA
BHTA
62
RADE
69
TO
BLI
DRIVER
60b
120a
ACTB
70
BLEQ
120b
63
71
SON
64
72
SOP
120c
73
ACTC
RXT
RST_B
67
120d
65
76
ACTLAT
60c
60d
60da
/PRCA
68
66
41
60db
PRCA
60e
74
PRCB

FIG.34

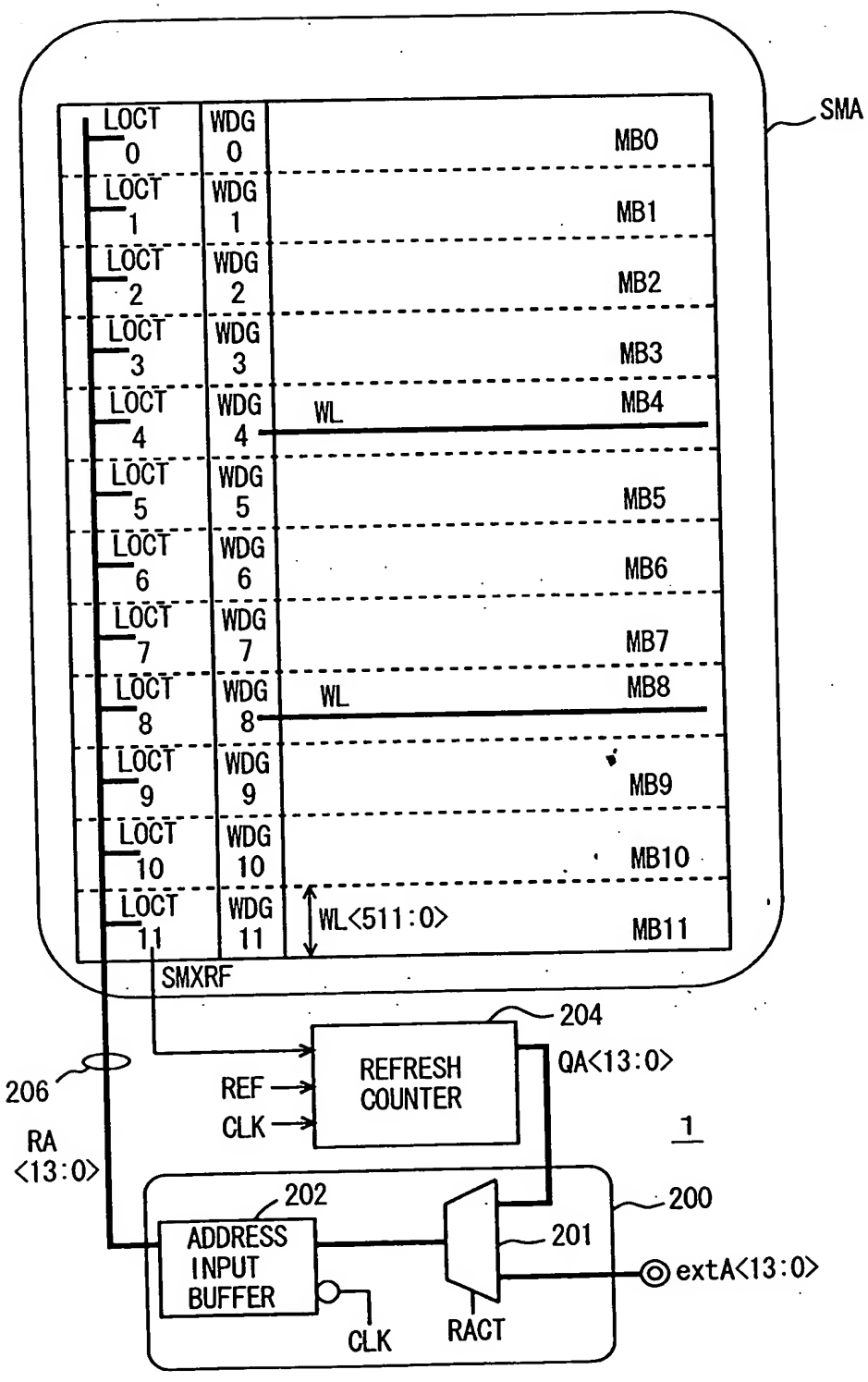

SMA
LOCT 0
WDG 0
MB0
LOCT 1
WDG 1
MB1
LOCT 2
WDG 2
MB2
LOCT 3
WDG 3
MB3
LOCT 4
WDG 4
WL
MB4
LOCT 5
WDG 5
MB5
LOCT 6
WDG 6
MB6
LOCT 7
WDG 7
MB7
LOCT 8
WDG 8
WL
MB8
LOCT 9
WDG 9
MB9
LOCT 10
WDG 10
MB10
LOCT 11
WDG 11
WL<511:0>
MB11
SMXRF
204
REFRESH COUNTER
QA<13:0>
206
REF
CLK
RA <13:0>
1
202
ADDRESS INPUT BUFFER
CLK
RACT
201
200
extA<13:0>

FIG.35

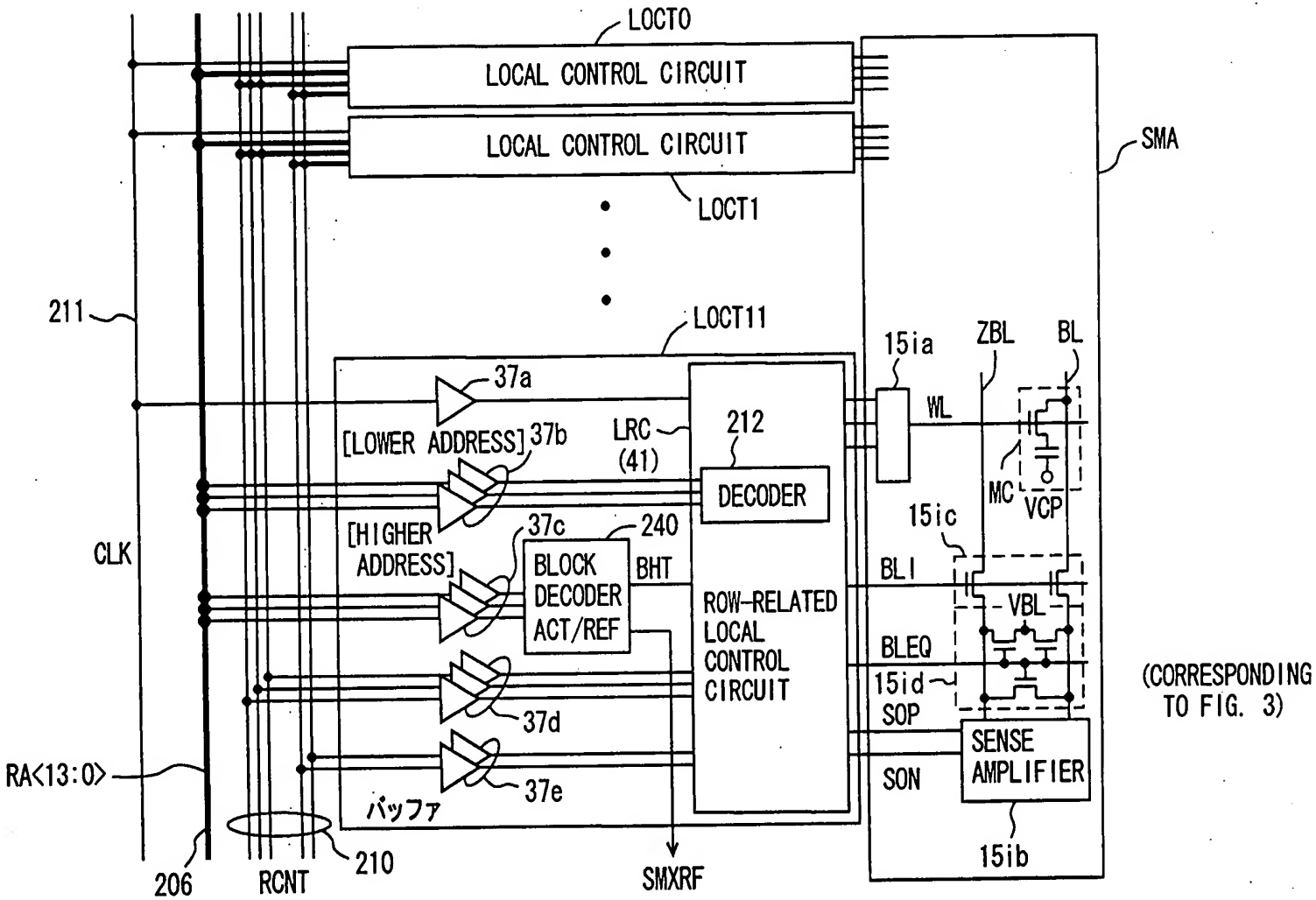

LOCT0
LOCAL CONTROL CIRCUIT
LOCAL CONTROL CIRCUIT
LOCT1
LOCT11
SMA
211
37a
[LOWER ADDRESS]
37b
LRC
(41)
212
DECODER
[HIGHER
ADDRESS]
37c
240
BLOCK
DECODER
ACT/REF
BHT
ROW-RELATED
LOCAL
CONTROL
CIRCUIT
CLK
37d
37e
バッファ
RA<13:0>
206
RCNT
210
SMXRF
15ia
ZBL
BL
WL
MC
VCP
15ic
BLI
VBL
BLEQ
15id
SOP
SON
SENSE
AMPLIFIER
15ib
(CORRESPONDING
TO FIG. 3)

FIG.36

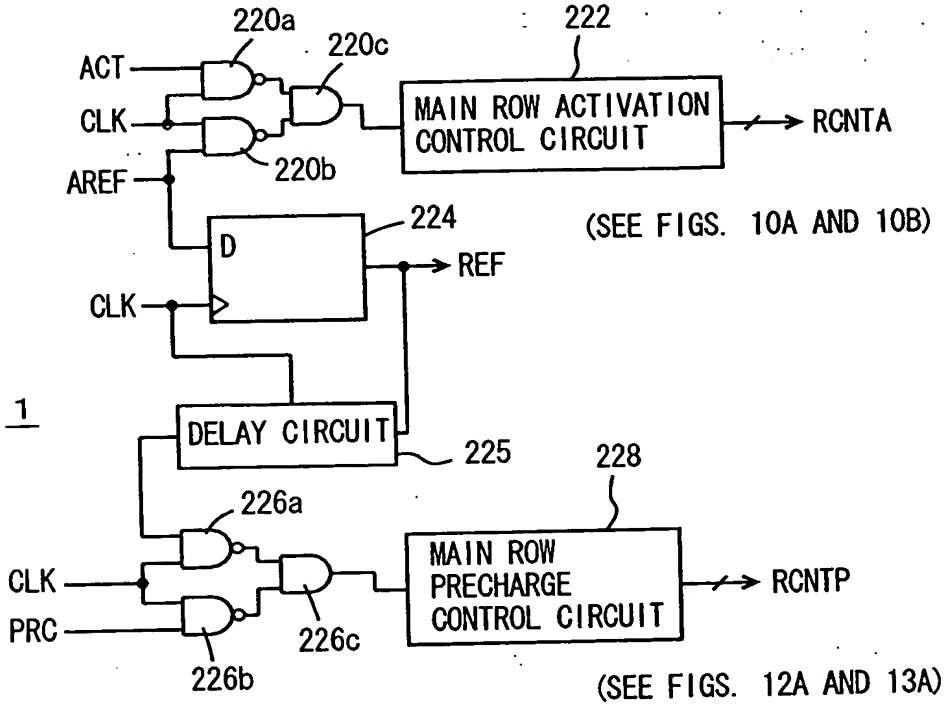

220a
220c
222
ACT
CLK
AREF
220b
MAIN ROW ACTIVATION CONTROL CIRCUIT
RCNTA
(SEE FIGS. 10A AND 10B)
224
D
REF
CLK
1
DELAY CIRCUIT
225
228
226a
CLK
PRC
226c
MAIN ROW PRECHARGE CONTROL CIRCUIT
RCNTP
226b
(SEE FIGS. 12A AND 13A)

FIG.37

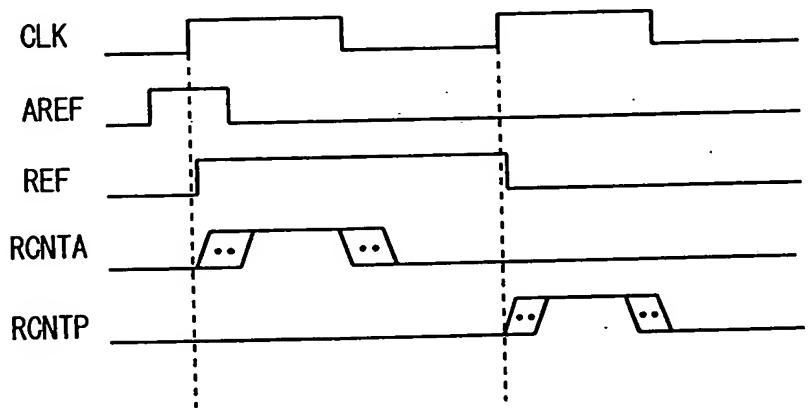

CLK
AREF
REF
RCNTA
RCNTP

FIG.38

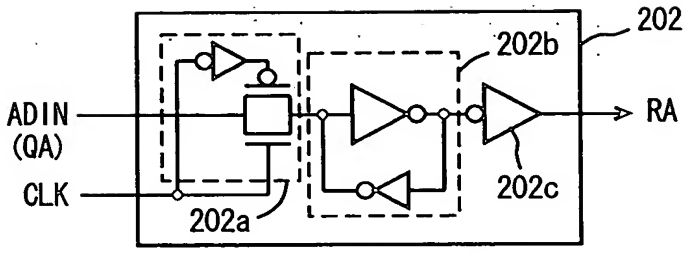



FIG.39

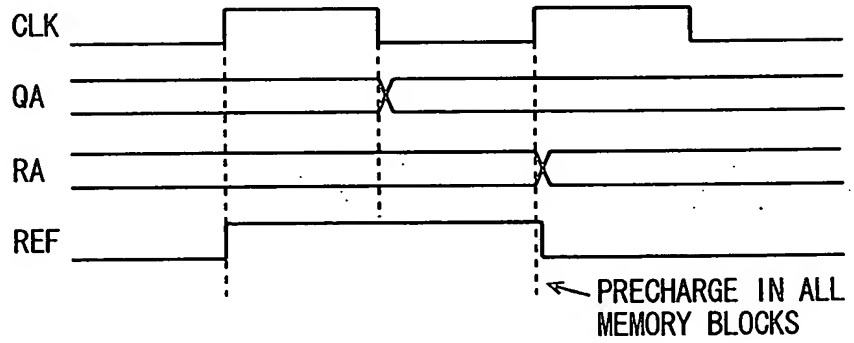



FIG.40

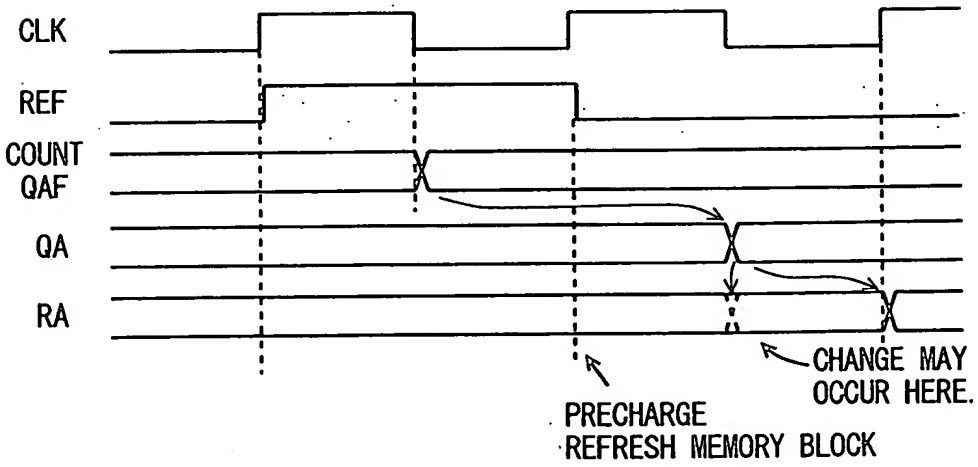


FIG.41

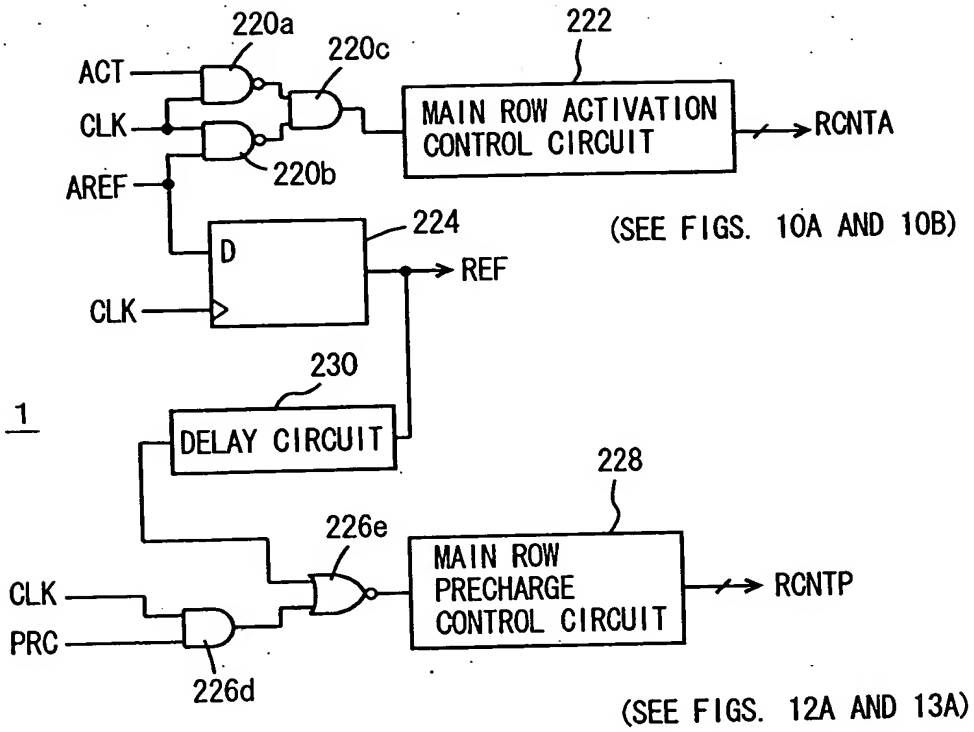

220a
220c
222
ACT
CLK
AREF
220b
MAIN ROW ACTIVATION CONTROL CIRCUIT
RCNTA
(SEE FIGS. 10A AND 10B)
224
D
REF
CLK
230
1
DELAY CIRCUIT
228
226e
MAIN ROW PRECHARGE CONTROL CIRCUIT
RCNTP
CLK
PRC
226d
(SEE FIGS. 12A AND 13A)

FIG.42

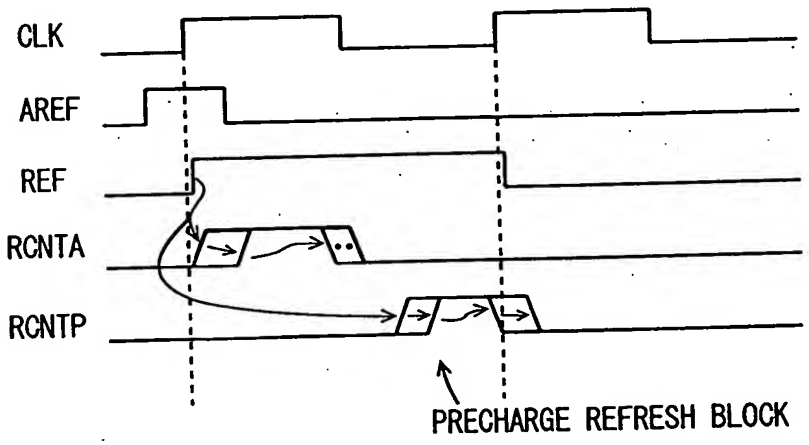

CLK
AREF
REF
RCNTA
RCNTP
PRECHARGE REFRESH BLOCK

FIG.43

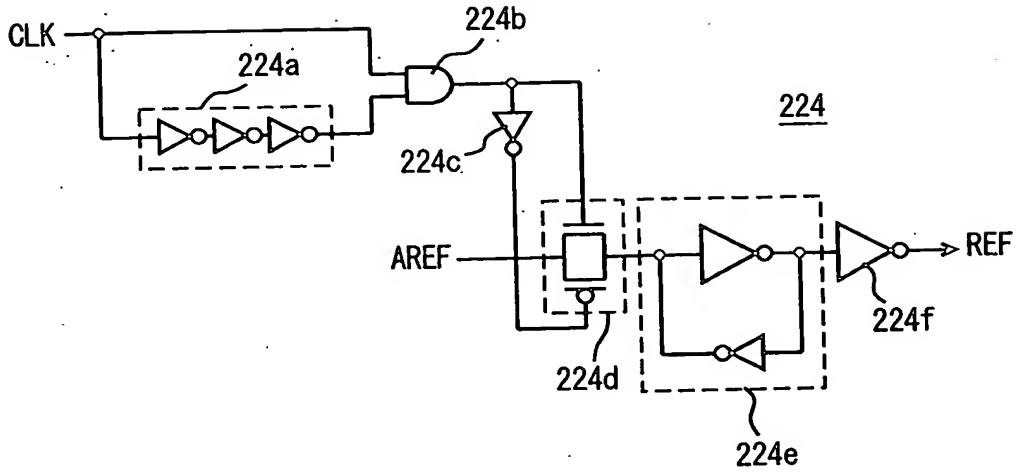

CLK
224a
224b
224
224c
AREF
REF
224f
224d
224e

FIG.45

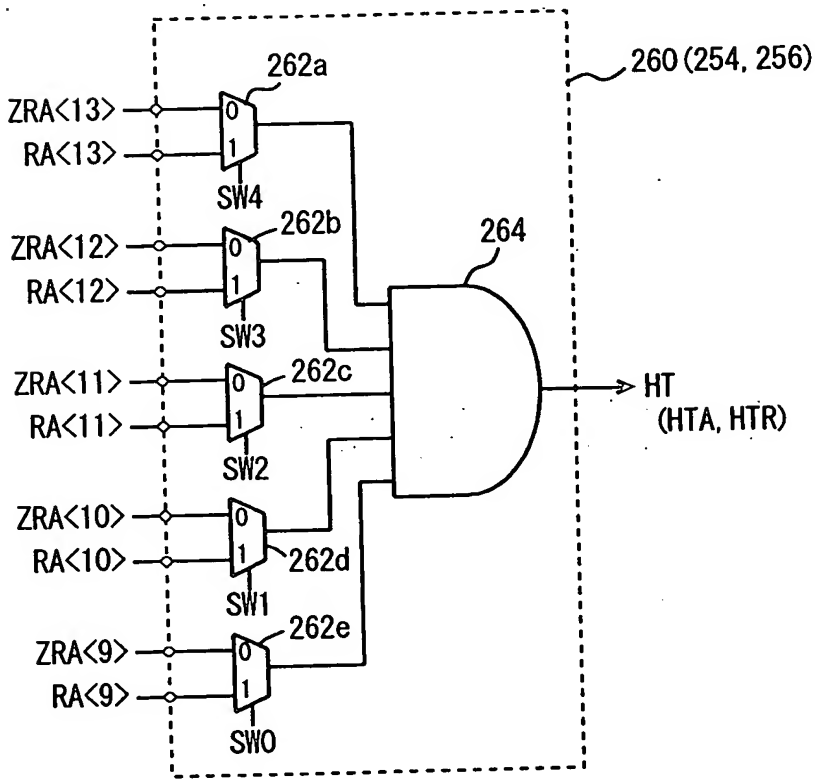

260 (254, 256)
262a
ZRA<13>
RA<13>
SW4
262b
ZRA<12>
RA<12>
SW3
264
262c
ZRA<11>
RA<11>
SW2
HT
(HTA, HTR)
ZRA<10>
RA<10>
SW1
262d
262e
ZRA<9>
RA<9>
SW0

FIG.44

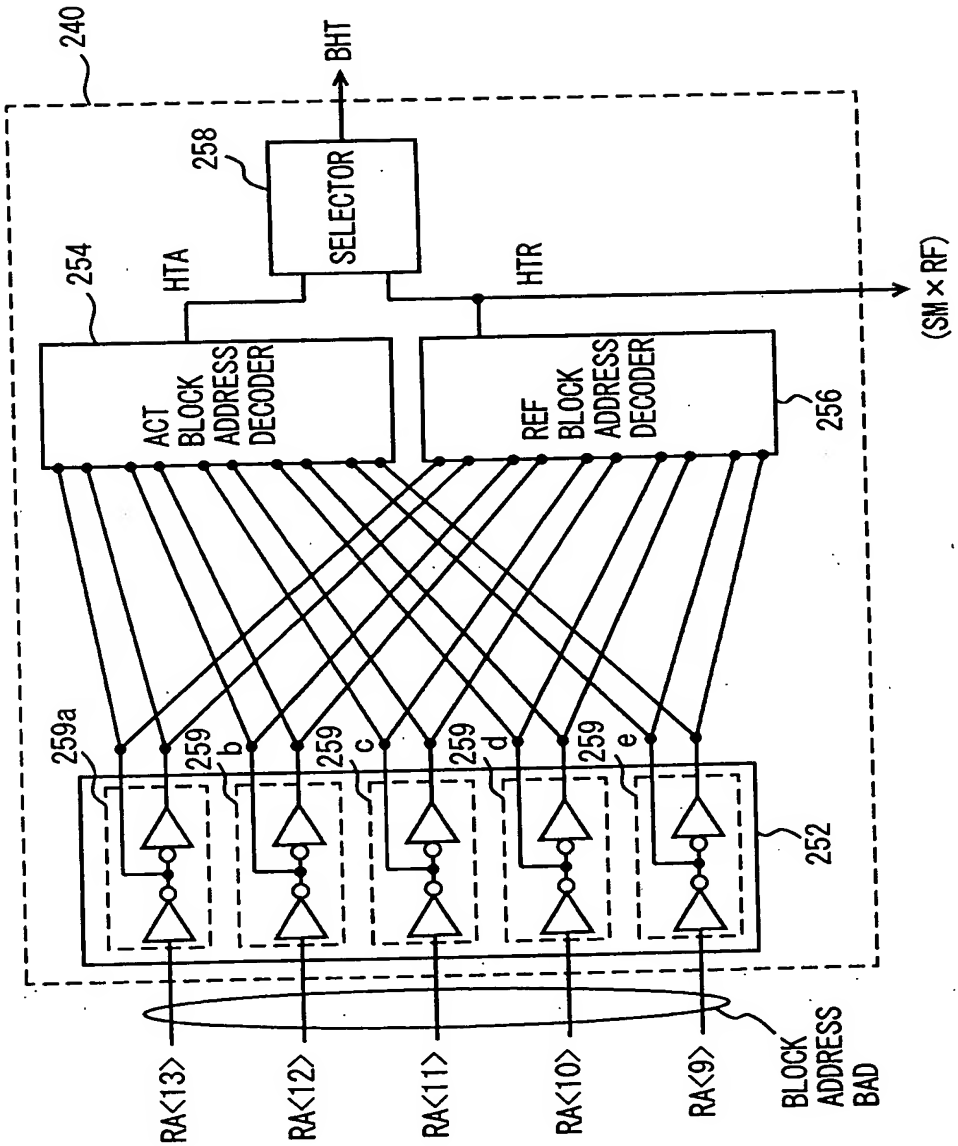

240
BHT
258
SELECTOR
254
HTA
HTR
(SM × RF)
ACT BLOCK ADDRESS DECODER
REF BLOCK ADDRESS DECODER
256
259a
259 b
259 c
259 d
259 e
252
RA<13>
RA<12>
RA<11>
RA<10>
RA<9>
BLOCK ADDRESS BAD

FIG.46

| MEMORY BLOCK MB | ACT BLOCK ADDRESS DECODER | | | | | REF BLOCK ADDRESS DECODER | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | SW4 | SW3 | SW2 | SW1 | SW0 | SW4 | SW3 | SW2 | SW1 | SW0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 5 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 6 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 8 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 9 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 10 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 11 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |

FIG.47

| MEMORY BLOCK MB | ACT BLOCK ADDRESS DECODER | | | | | REF BLOCK ADDRESS DECODER | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | SW4 | SW3 | SW2 | SW1 | SW0 | SW4 | SW3 | SW2 | SW1 | SW0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

FIG.48A

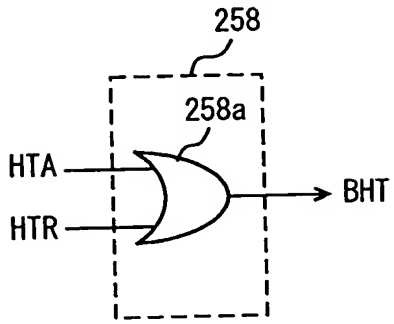



FIG.48B

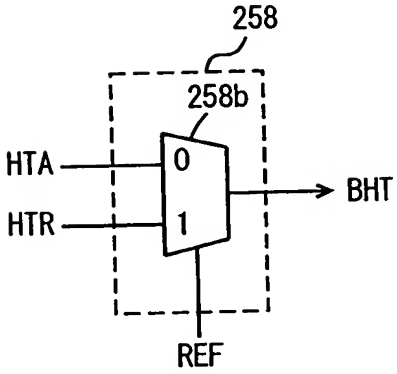



FIG.48C

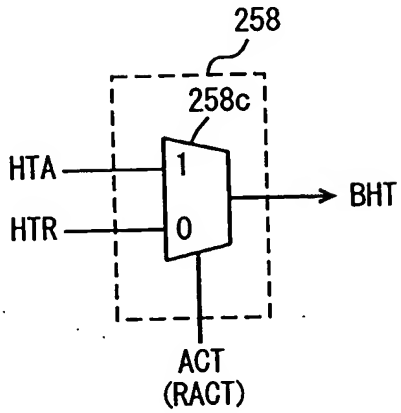


FIG.49

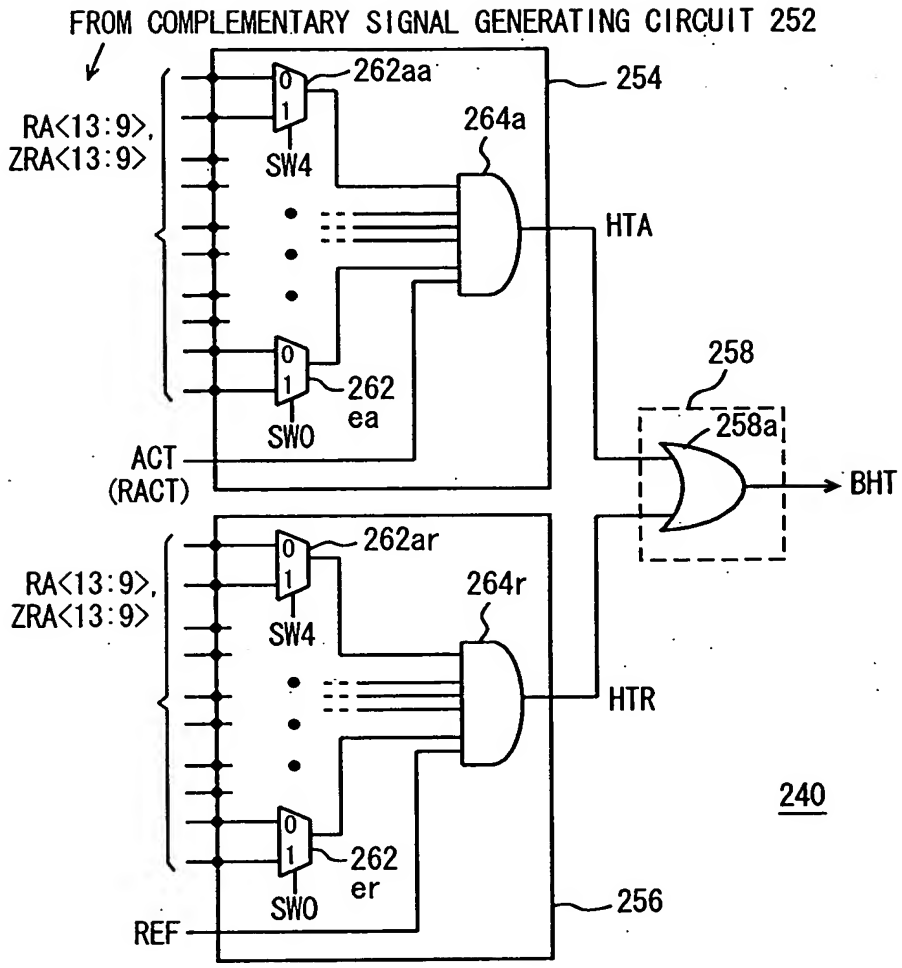

FROM COMPLEMENTARY SIGNAL GENERATING CIRCUIT 252
RA<13:9>,
ZRA<13:9>
SW4
262aa
254
264a
HTA
258
258a
262
ea
SW0
ACT
(RACT)
BHT
RA<13:9>,
ZRA<13:9>
SW4
262ar
264r
HTR
240
262
er
SW0
REF
256

FIG.50

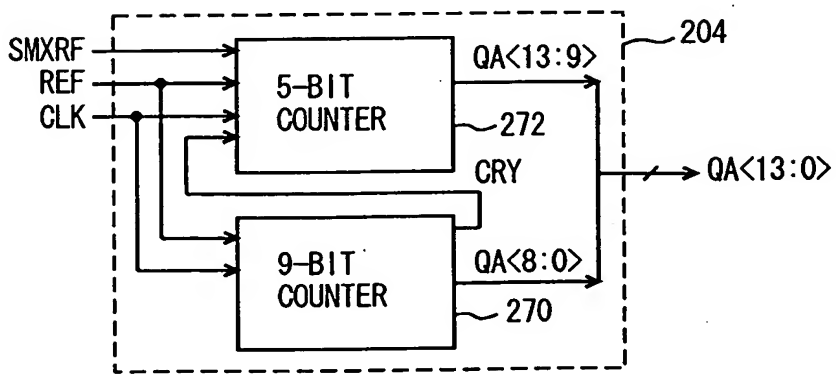

SMXRF
REF
CLK
5-BIT
COUNTER
QA<13:9>
272
CRY
204
QA<13:0>
9-BIT
COUNTER
QA<8:0>
270

FIG.51

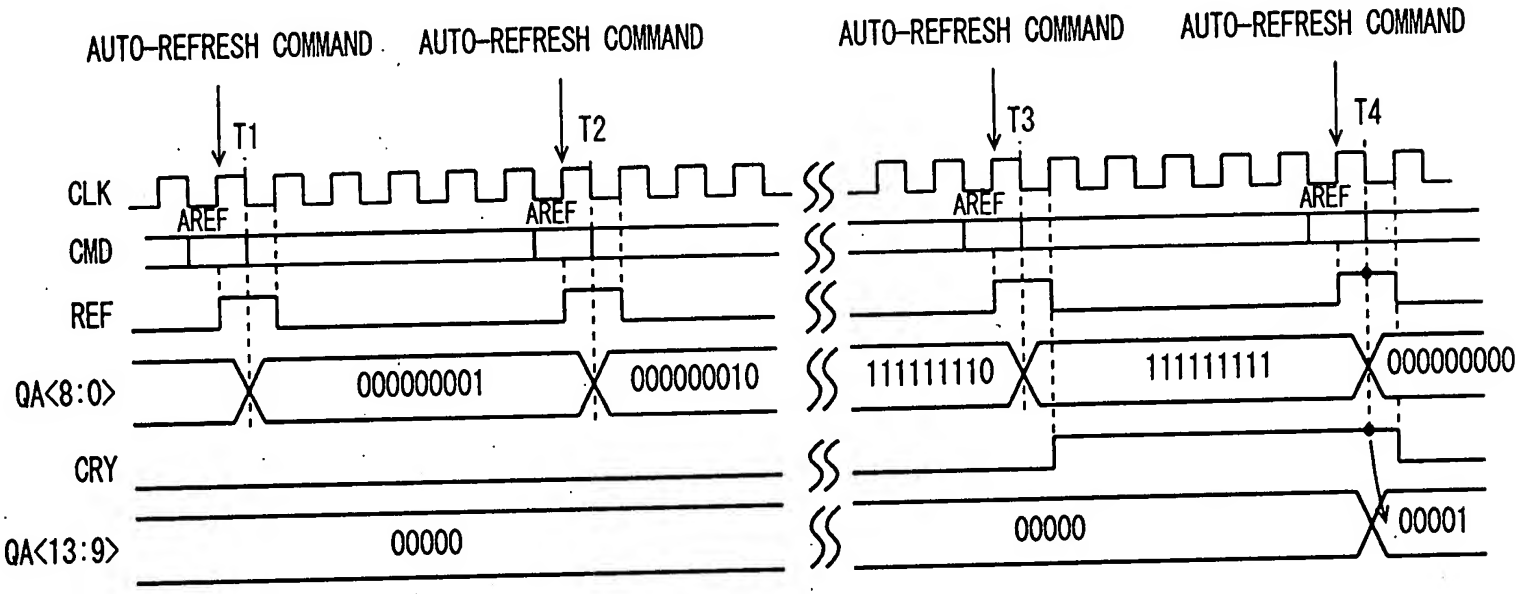

AUTO-REFRESH COMMAND
AUTO-REFRESH COMMAND
AUTO-REFRESH COMMAND
AUTO-REFRESH COMMAND
T1
T2
T3
T4
CLK
CMD
REF
QA<8:0>
CRY
QA<13:9>
AREF
AREF
AREF
AREF
000000001
000000010
111111110
111111111
000000000
00000
00000
00001

FIG.52

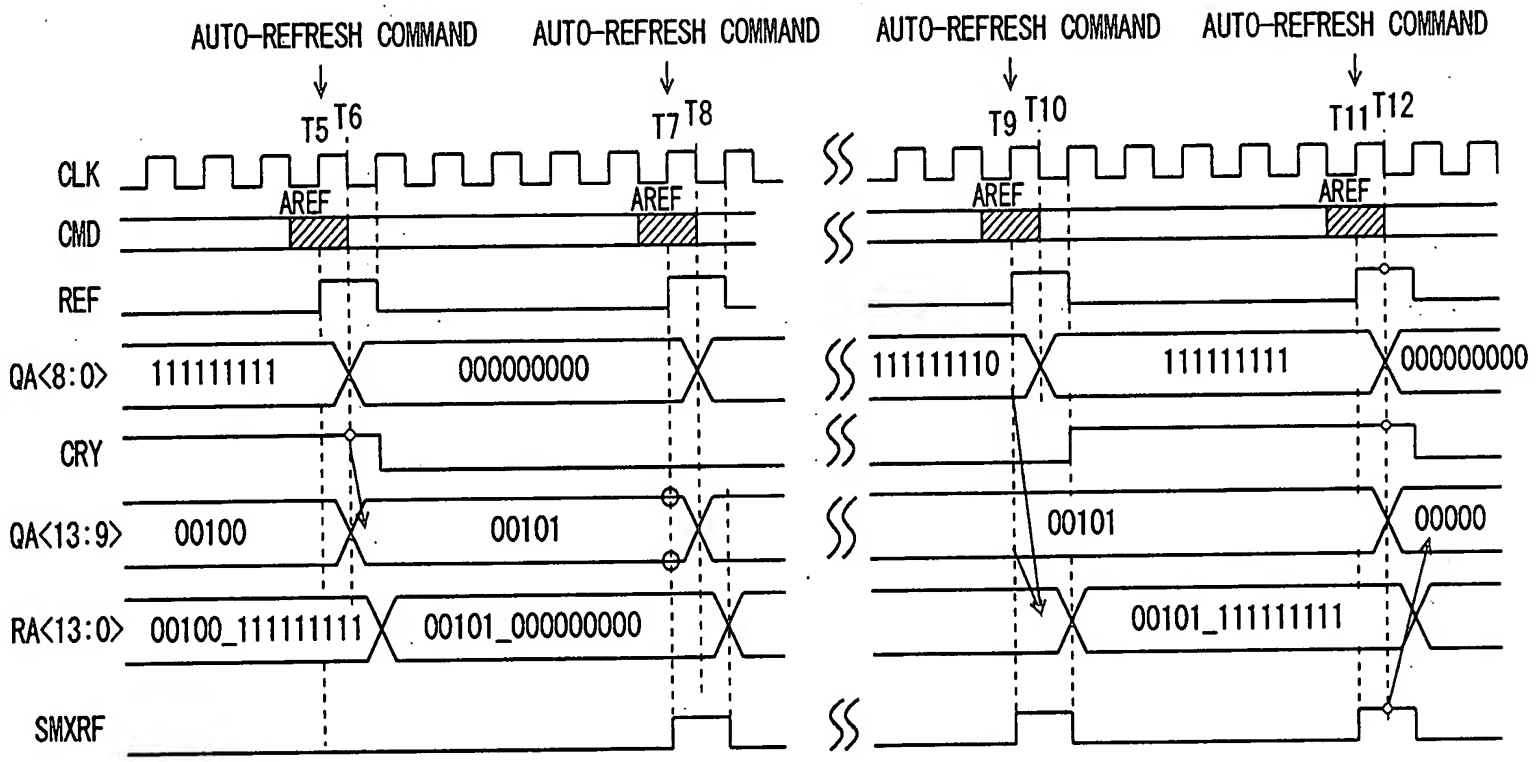

AUTO-REFRESH COMMAND
AUTO-REFRESH COMMAND
AUTO-REFRESH COMMAND
AUTO-REFRESH COMMAND
T5
T6
T7
T8
T9
T10
T11
T12
CLK
CMD
REF
QA<8:0>
CRY
QA<13:9>
RA<13:0>
SMXRF
AREF
AREF
AREF
AREF
111111111
000000000
111111110
111111111
000000000
00100
00101
00101
00000
00100_111111111
00101_000000000
00101_111111111

FIG.53

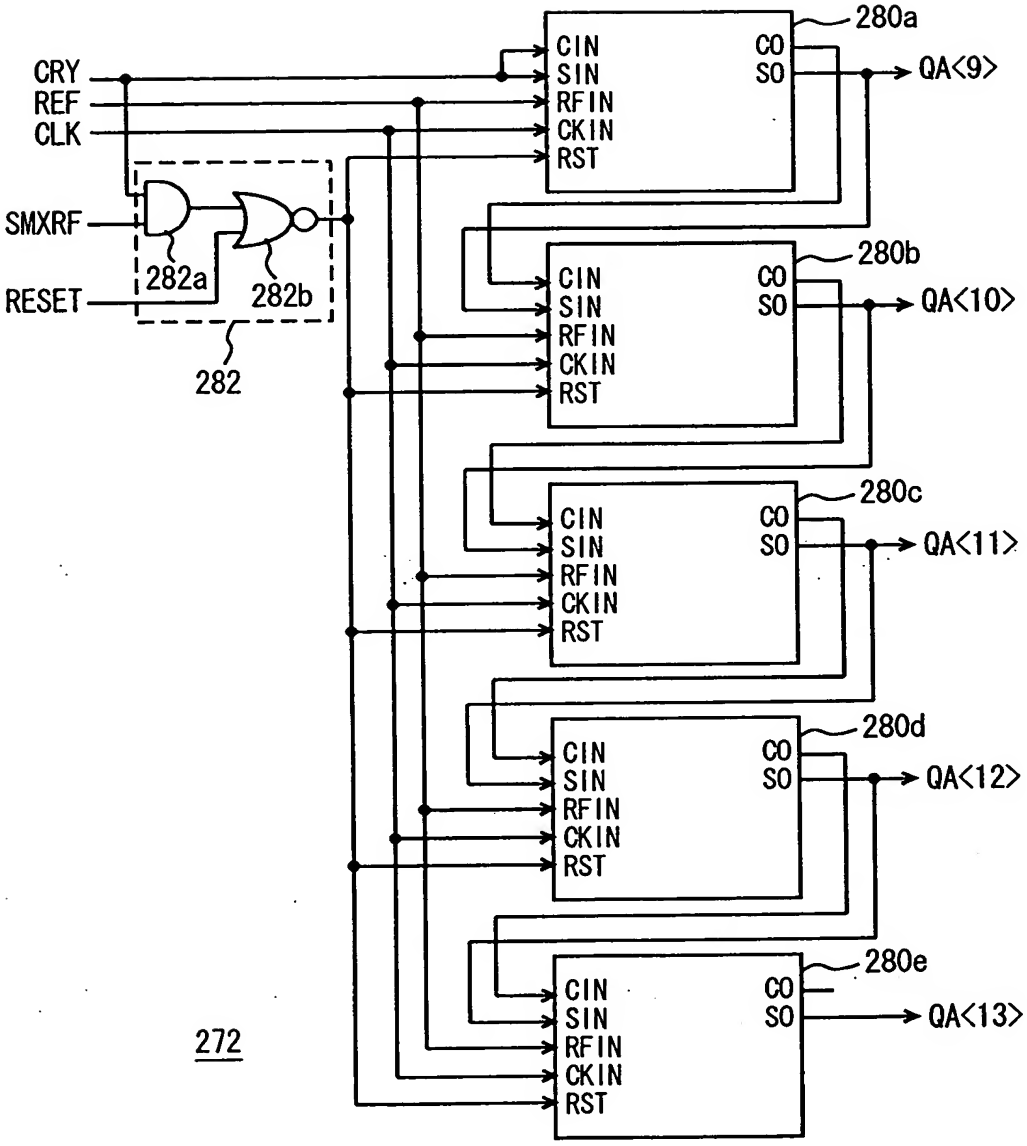

CRY
REF
CLK
SMXRF
RESET
282a
282b
282
272
280a
280b
280c
280d
280e
CIN
SIN
RFIN
CKIN
RST
CO
SO
QA<9>
QA<10>
QA<11>
QA<12>
QA<13>

FIG.54

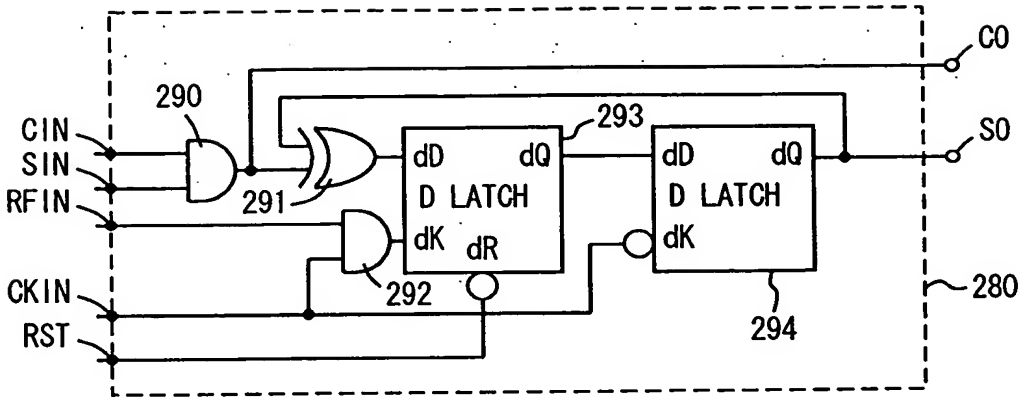



FIG.55

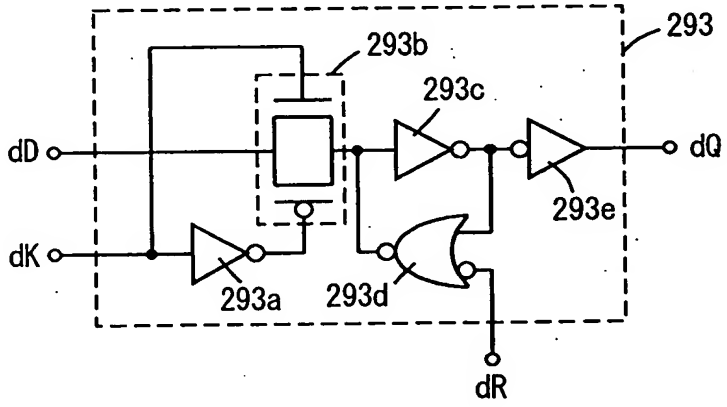



FIG.56

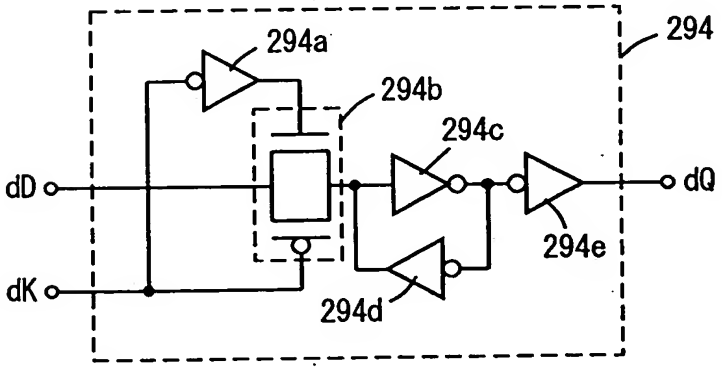


FIG.57

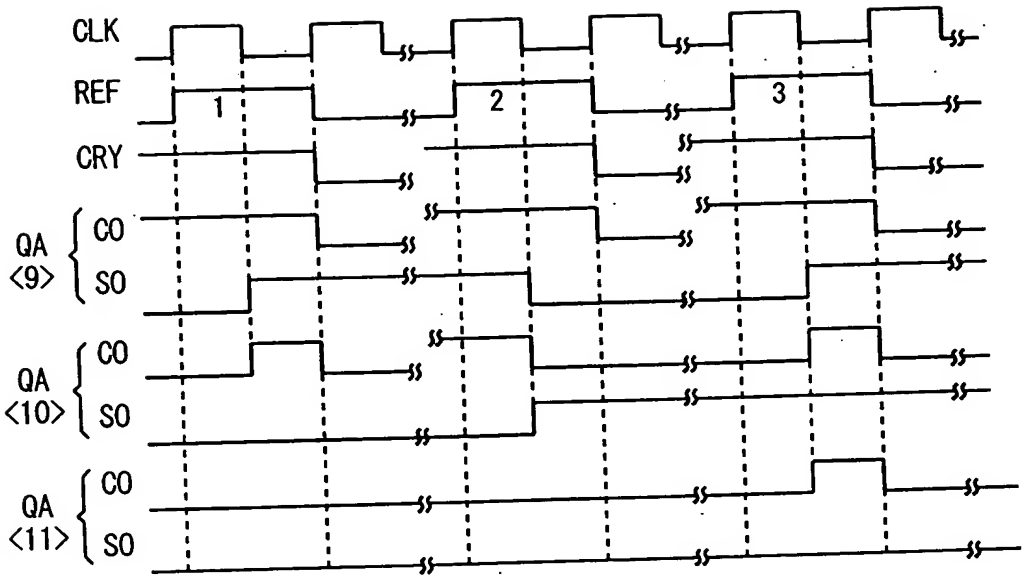

CLK
REF
CRY
QA <9>
CO
SO
QA <10>
CO
SO
QA <11>
CO
SO
1
2
3

FIG.58

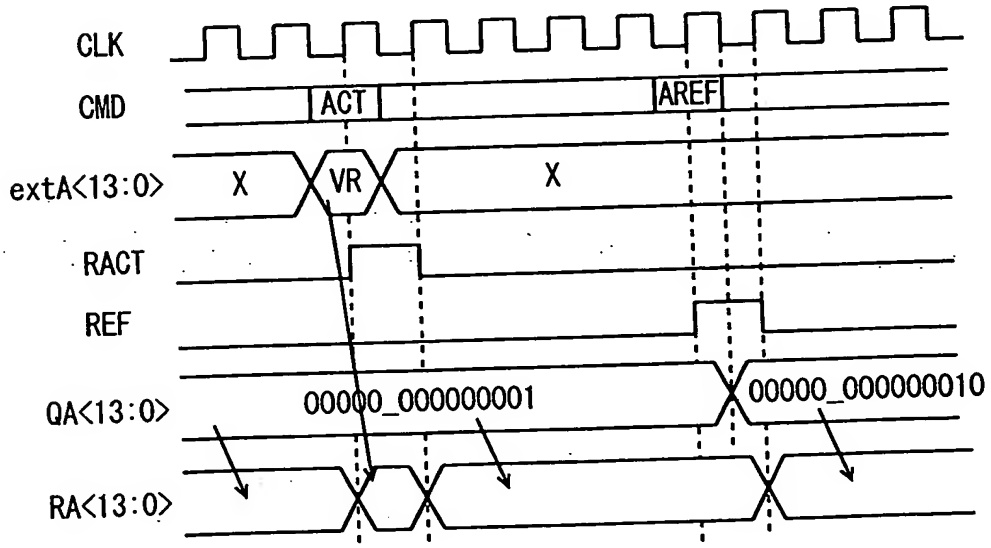

CLK
CMD
ACT
AREF
extA<13:0>
X
VR
X
RACT
REF
QA<13:0>
00000_000000001
00000_000000010
RA<13:0>

FIG.59

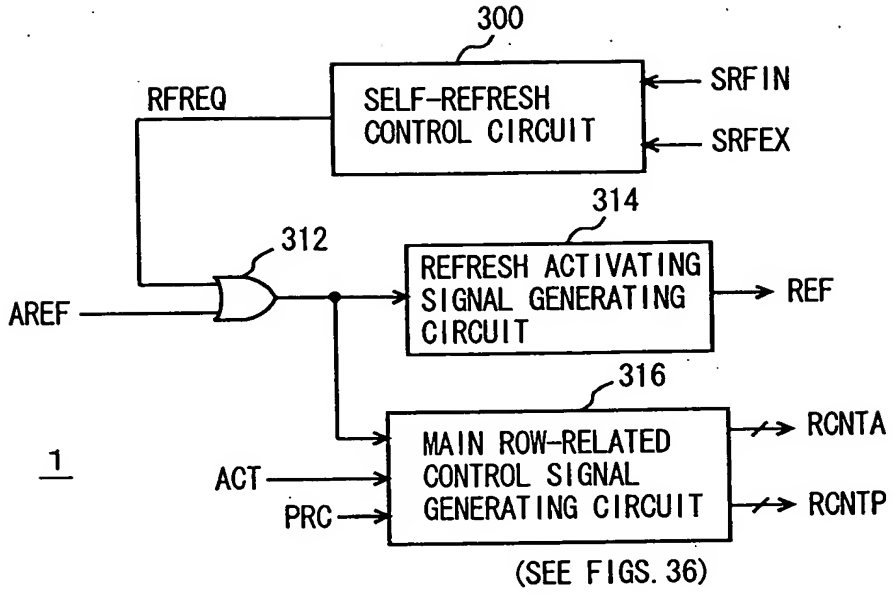

300
SELF-REFRESH CONTROL CIRCUIT
SRFIN
SRFEX
RFREQ
314
312
REFRESH ACTIVATING SIGNAL GENERATING CIRCUIT
REF
AREF
316
MAIN ROW-RELATED CONTROL SIGNAL GENERATING CIRCUIT
RCNTA
RCNTP
ACT
PRC
1
(SEE FIGS. 36)

FIG.60

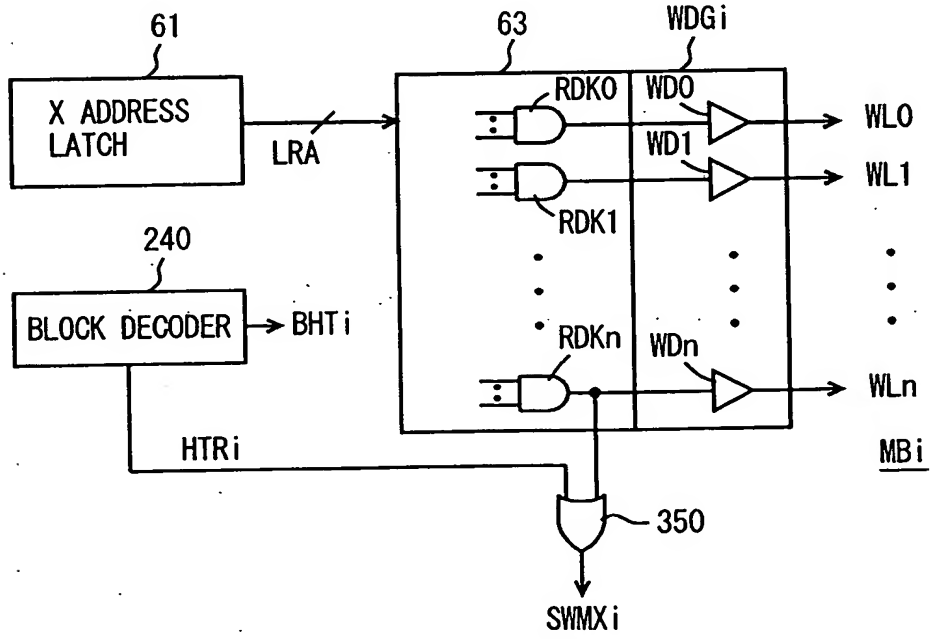

61
X ADDRESS LATCH
LRA
63
WDGi
RDK0
WD0
WL0
WD1
WL1
RDK1
240
BLOCK DECODER
BHTi
RDKn
WDn
WLn
MBi
HTRi
350
SWMXi

FIG.61

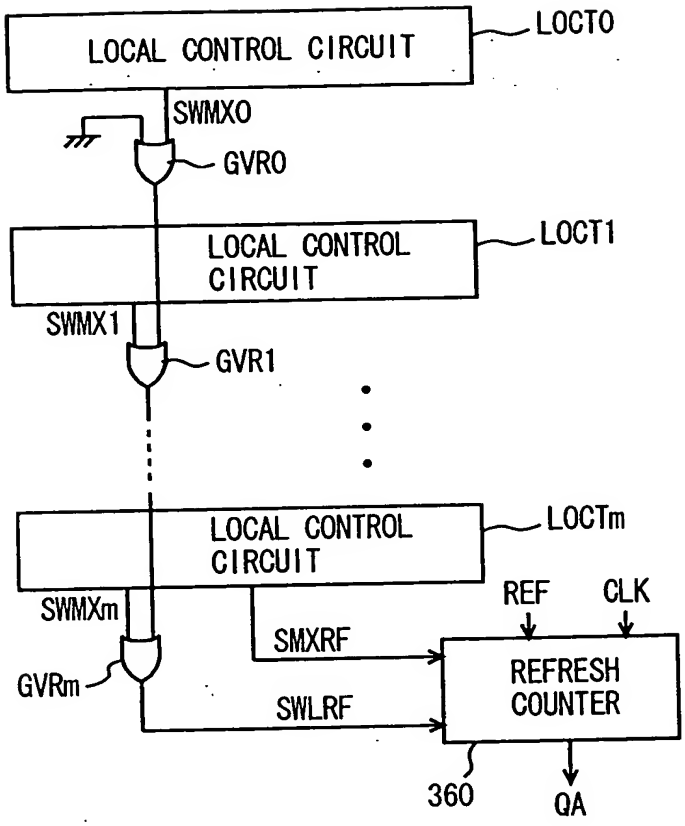

LOCAL CONTROL CIRCUIT
LOCT0
SWMX0
GVR0
LOCAL CONTROL CIRCUIT
LOCT1
SWMX1
GVR1
LOCAL CONTROL CIRCUIT
LOCTm
SWMXm
GVRm
REF
CLK
SMXRF
SWLRF
REFRESH COUNTER
360
QA

FIG.62

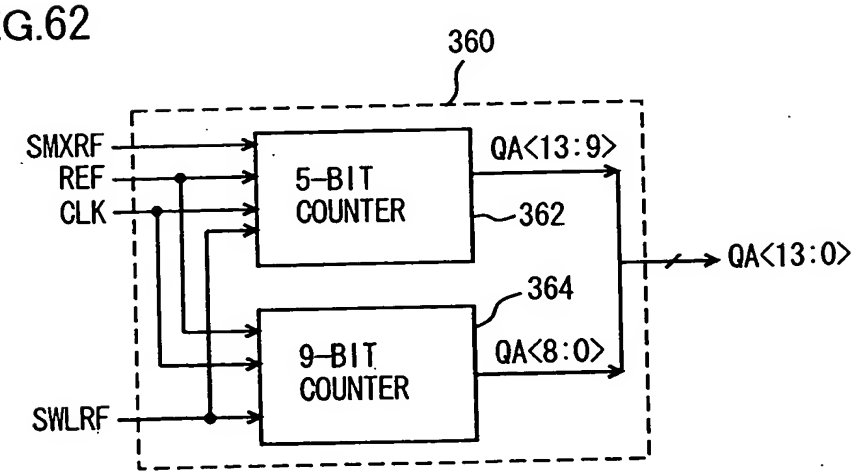

360
SMXRF
REF
CLK
5-BIT COUNTER
QA<13:9>
362
QA<13:0>
364
9-BIT COUNTER
QA<8:0>
SWLRF

FIG.63

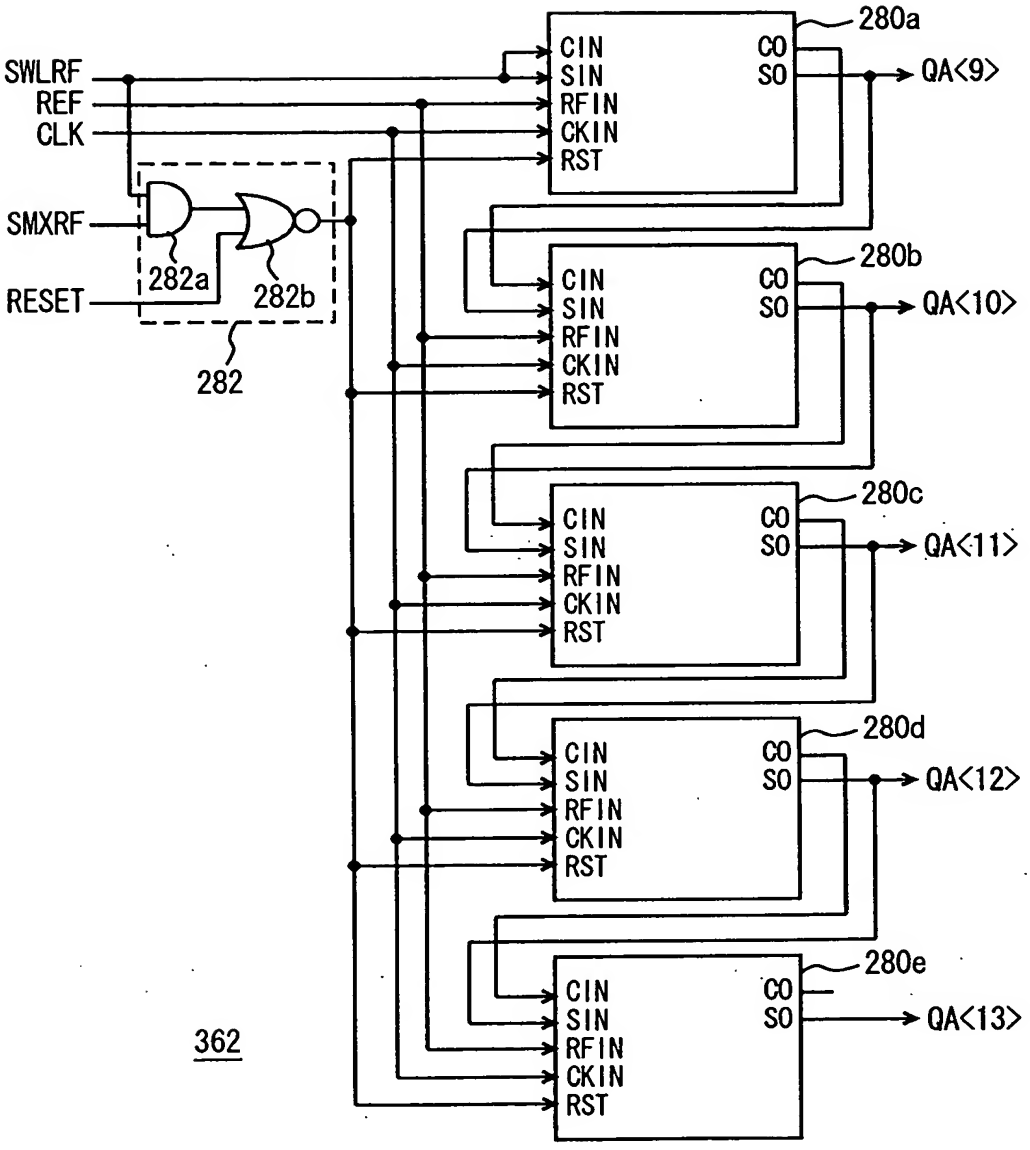

SWLRF
REF
CLK
SMXRF
RESET
282a
282b
282
362
280a
280b
280c
280d
280e
CIN
SIN
RFIN
CKIN
RST
CO
SO
QA<9>
QA<10>
QA<11>
QA<12>
QA<13>

FIG.64

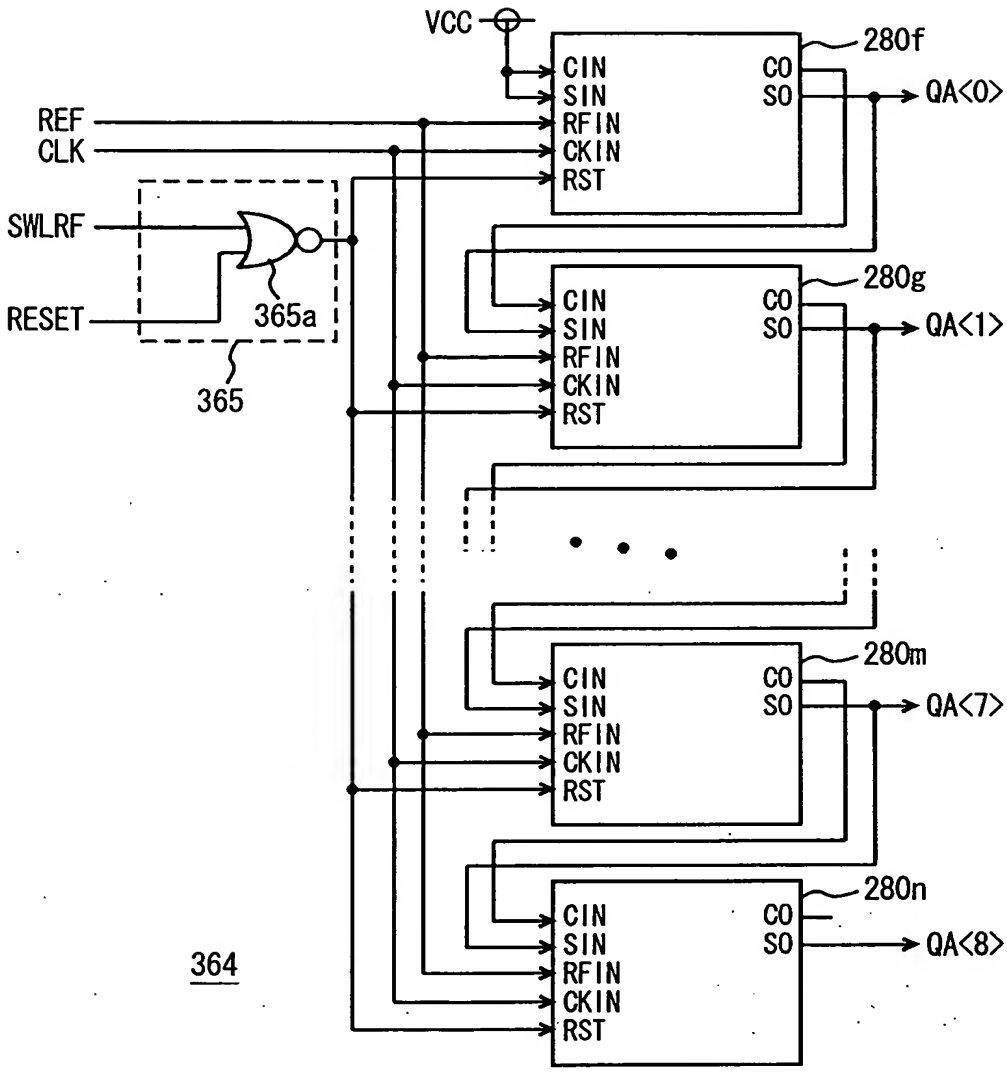

VCC
280f
CIN
SIN
RFIN
CKIN
RST
CO
SO
QA<0>
REF
CLK
SWLRF
RESET
365a
365
280g
QA<1>
280m
QA<7>
280n
QA<8>
364

FIG.65

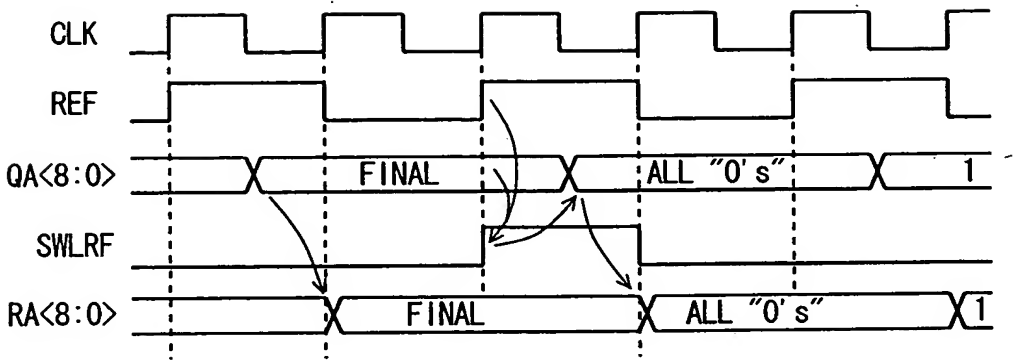

CLK
REF
QA<8:0>
FINAL
ALL "0's"
1
SWLRF
RA<8:0>
FINAL
ALL "0's"
1

FIG.66

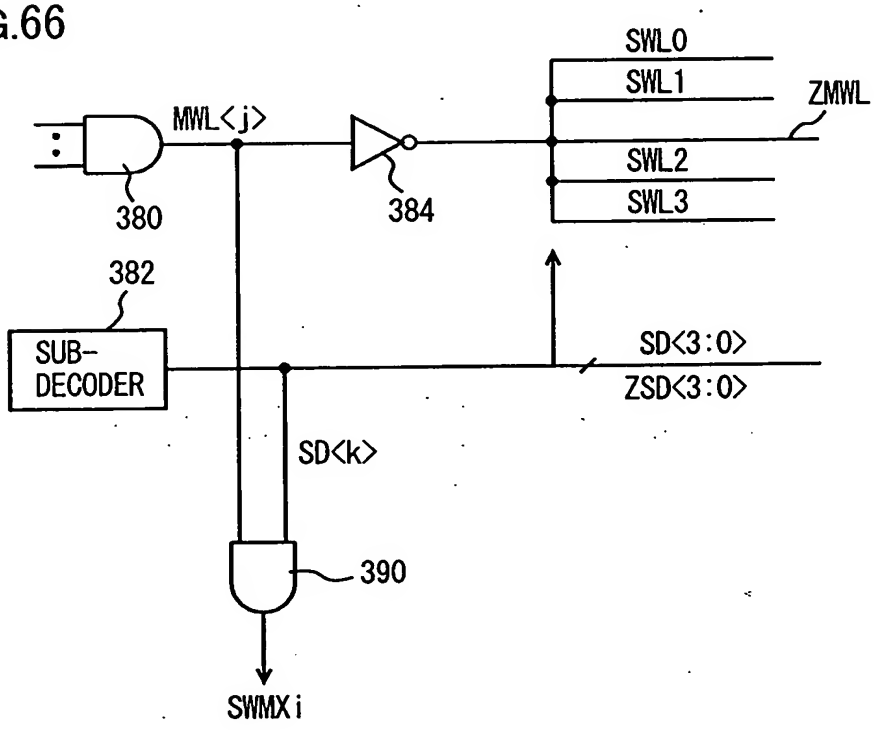

SWL0
SWL1
ZMWL
MWL<j>
SWL2
SWL3
380
384
382
SUB-
DECODER
SD<3:0>
ZSD<3:0>
SD<k>
390
SWMXi

FIG.67

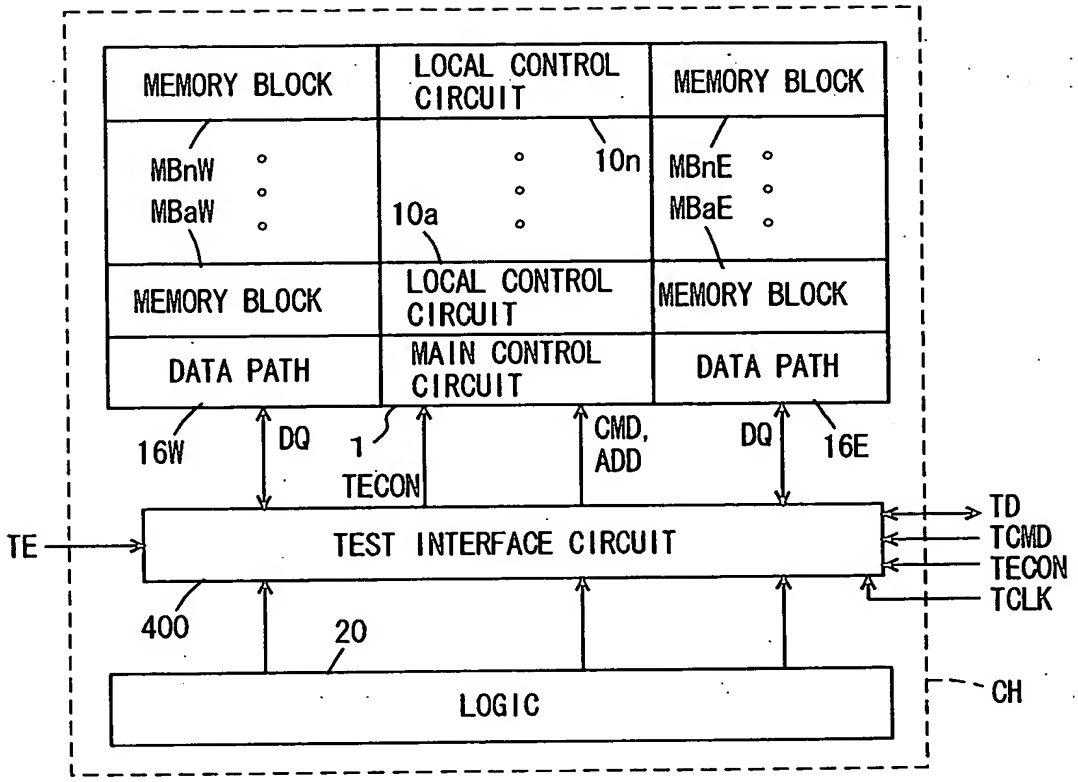

MEMORY BLOCK
LOCAL CONTROL CIRCUIT
MEMORY BLOCK
MBnW
MBaW
10n
10a
MBnE
MBaE
MEMORY BLOCK
LOCAL CONTROL CIRCUIT
MEMORY BLOCK
DATA PATH
MAIN CONTROL CIRCUIT
DATA PATH
16W
DQ
1
TECON
CMD, ADD
DQ
16E
TE
TEST INTERFACE CIRCUIT
TD
TCMD
TECON
TCLK
400
20
LOGIC
CH

FIG.68

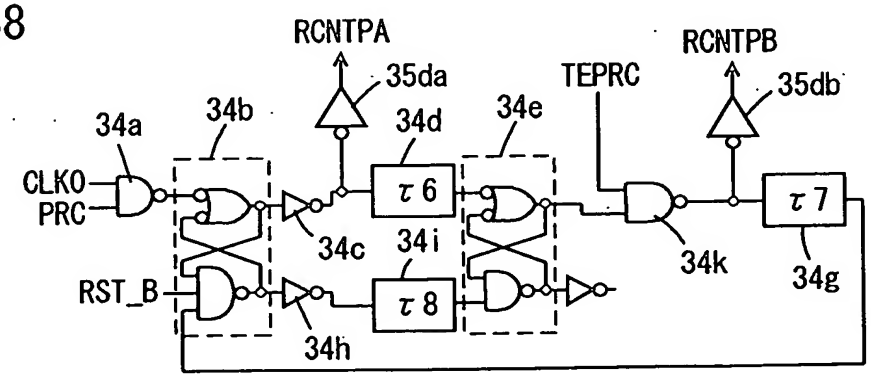

RCNTPA
35da
34a
34b
34d
34e
TEPRC
RCNTPB
35db
CLK0
PRC
τ 6
34c
34i
34k
τ 7
34g
RST_B
τ 8
34h
34

FIG.69

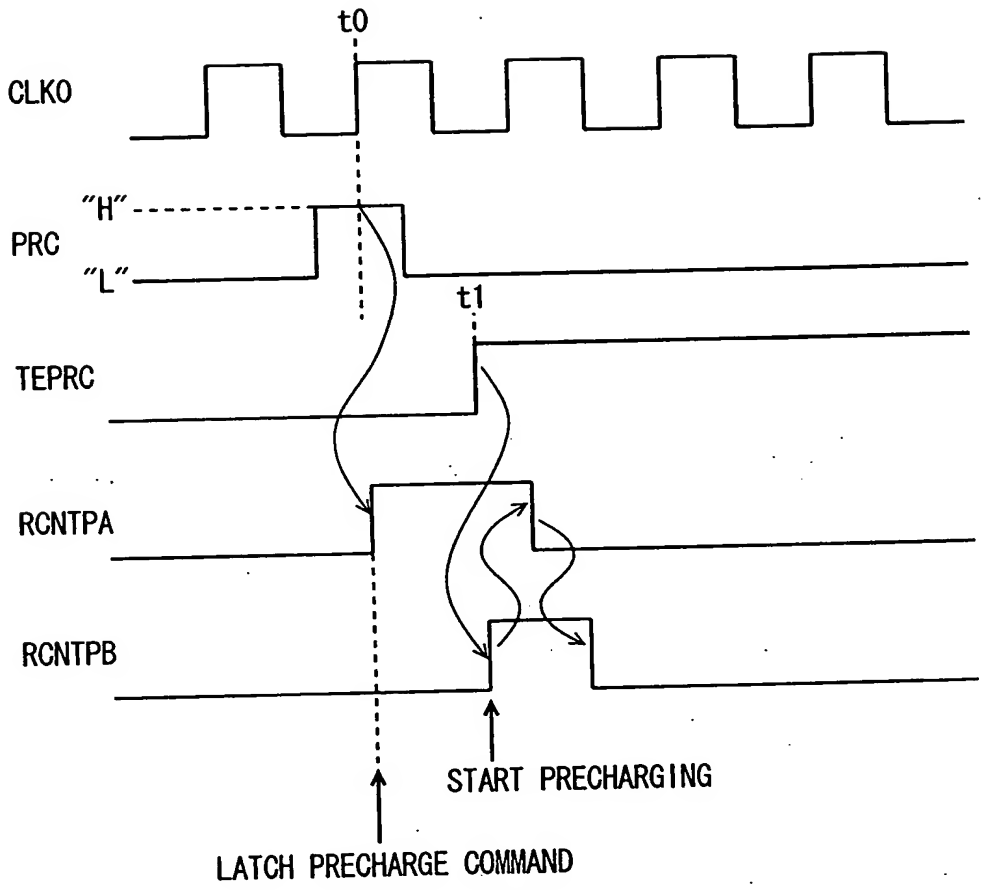

t0
CLKO
"H"
PRC
"L"
t1
TEPRC
RCNTPA
RCNTPB
START PRECHARGING
LATCH PRECHARGE COMMAND

FIG.70

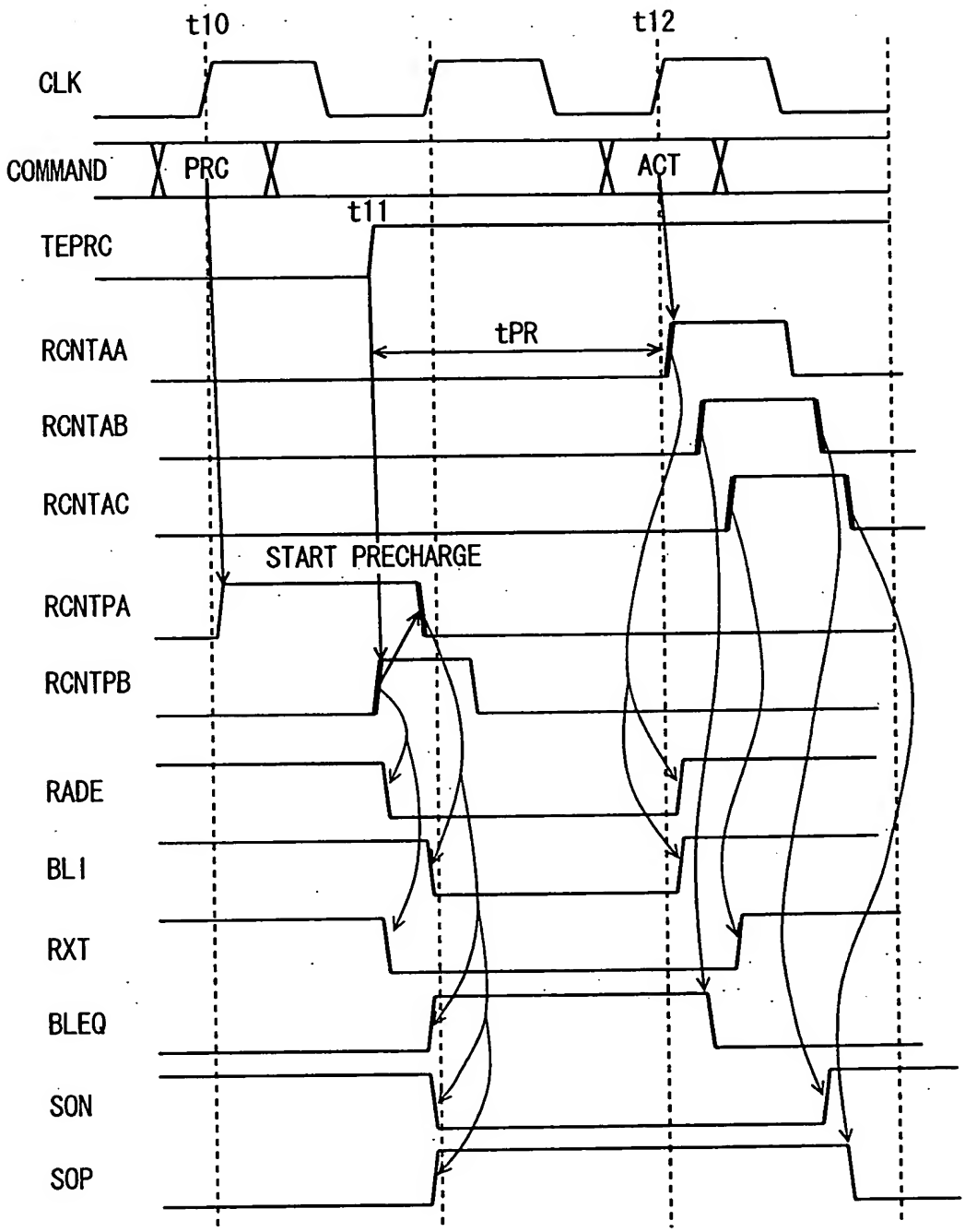

t10
t12
CLK
COMMAND
PRC
ACT
t11
TEPRC
tPR
RCNTAA
RCNTAB
RCNTAC
START PRECHARGE
RCNTPA
RCNTPB
RADE
BLI
RXT
BLEQ
SON
SOP

FIG.71

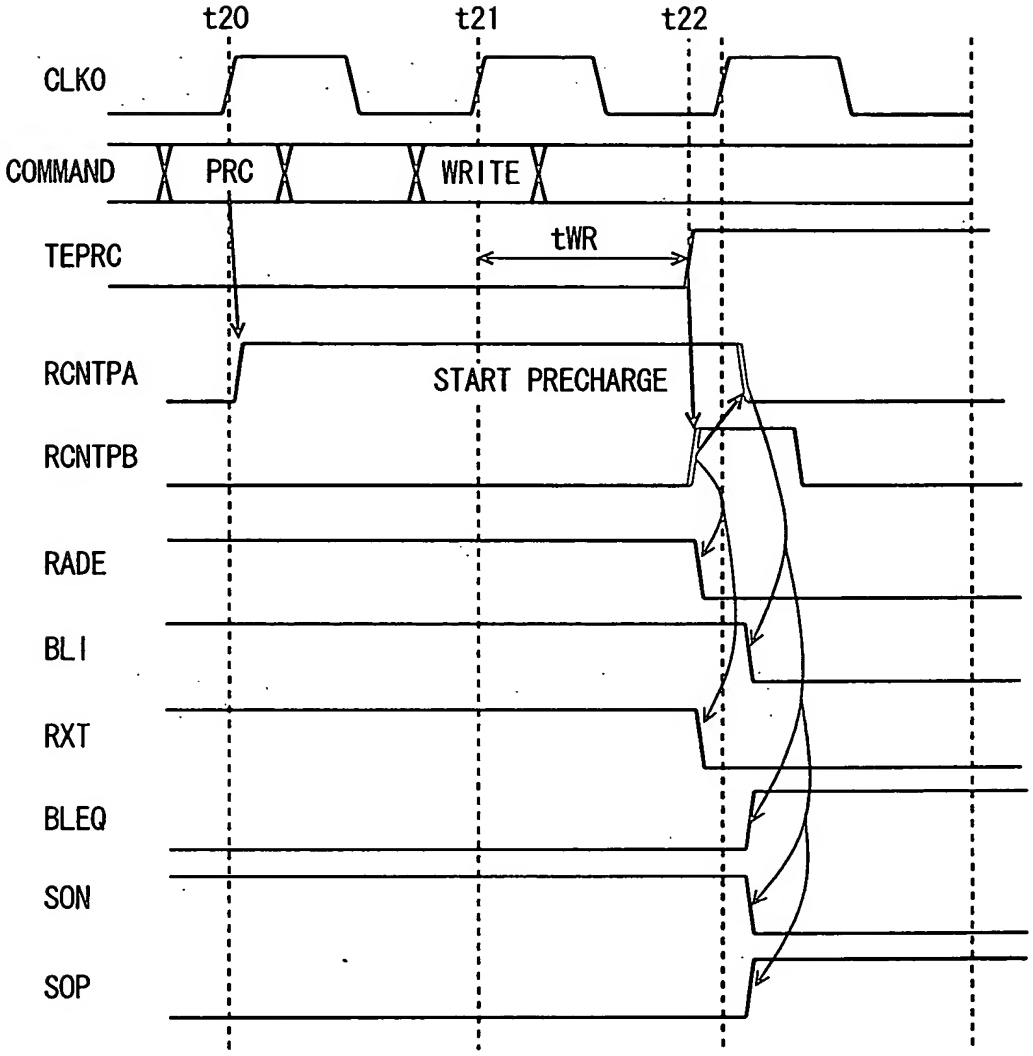

t20
t21
t22
CLKO
COMMAND
PRC
WRITE
TEPRC
tWR
RCNTPA
START PRECHARGE
RCNTPB
RADE
BLI
RXT
BLEQ
SON
SOP

FIG.72

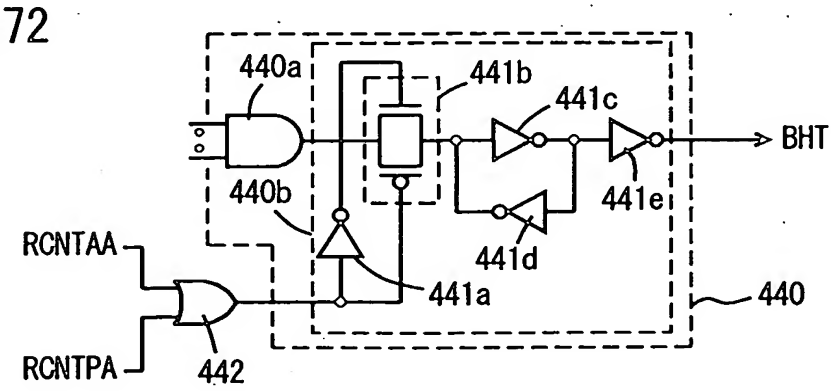

440a
441b
441c
BHT
440b
441e
441d
RCNTAA
441a
440
RCNTPA
442

FIG.73

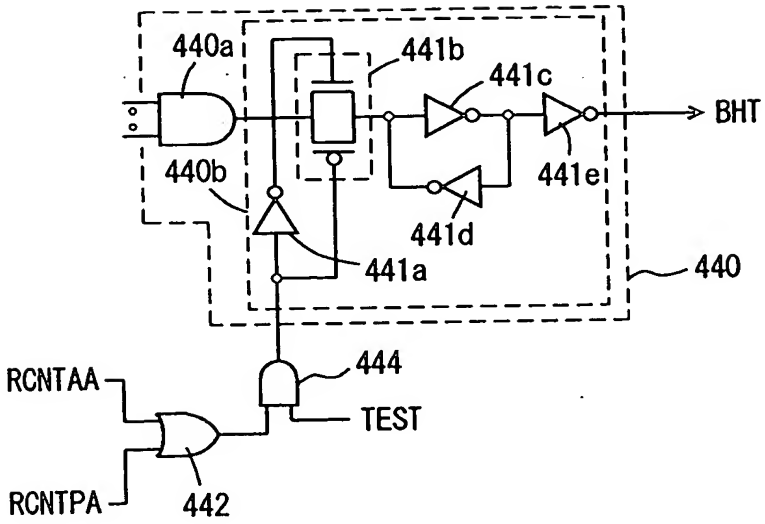

440a
441b
441c
BHT
440b
441e
441d
441a
440
444
RCNTAA
TEST
RCNTPA
442

FIG.74

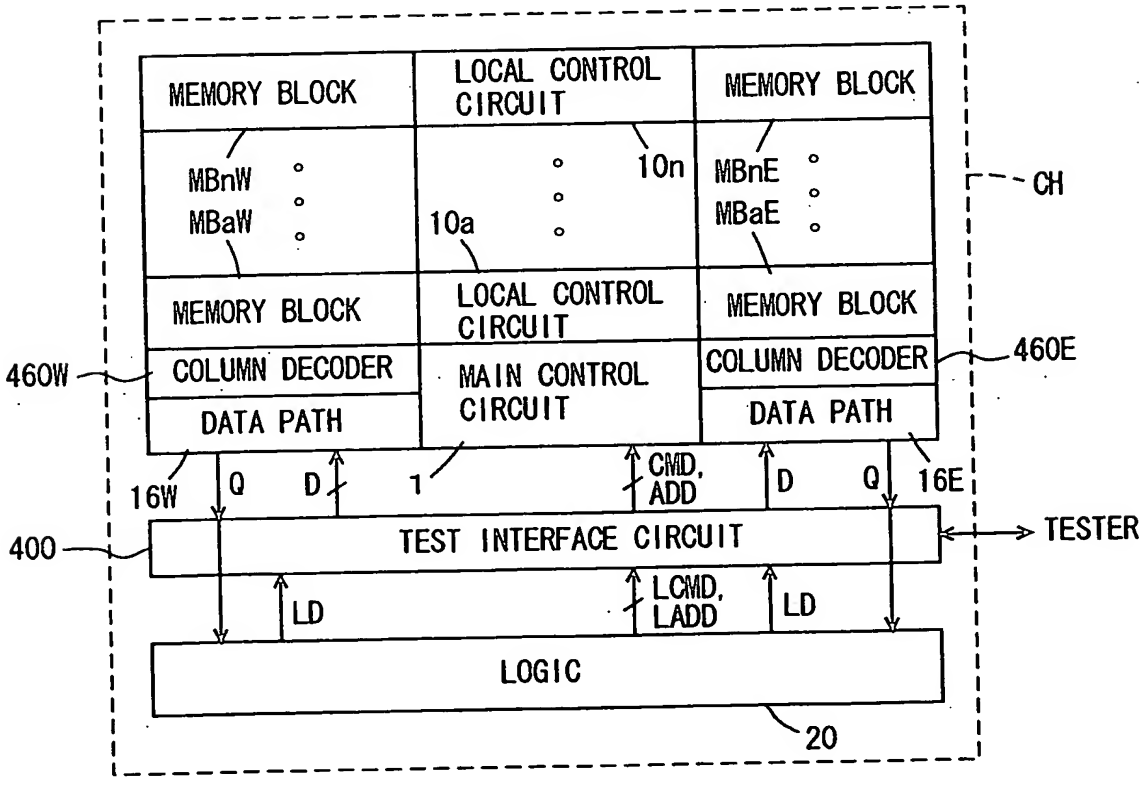

MEMORY BLOCK
LOCAL CONTROL CIRCUIT
MEMORY BLOCK
MBnW
MBaW
10n
10a
MBnE
MBaE
CH
MEMORY BLOCK
LOCAL CONTROL CIRCUIT
MEMORY BLOCK
460W
COLUMN DECODER
MAIN CONTROL CIRCUIT
COLUMN DECODER
460E
DATA PATH
DATA PATH
16W
Q
D
1
CMD, ADD
D
Q
16E
400
TEST INTERFACE CIRCUIT
TESTER
LD
LCMD, LADD
LD
LOGIC
20

FIG.75

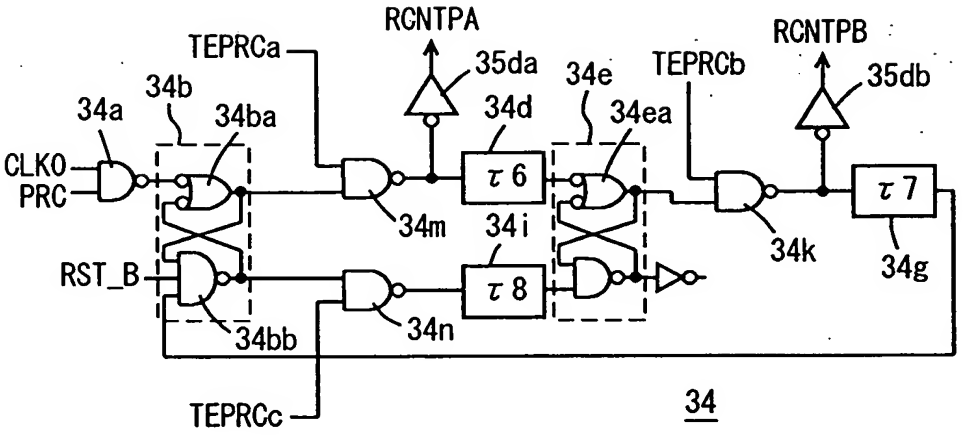

RCNTPA
RCNTPB
TEPRCa
35da
34e
TEPRCb
35db
34b
34d
34ea
34a
34ba
CLKO
PRC
τ 6
τ 7
34m
34i
34k
34g
RST_B
τ 8
34bb
34n
TEPRCc
34

FIG.76

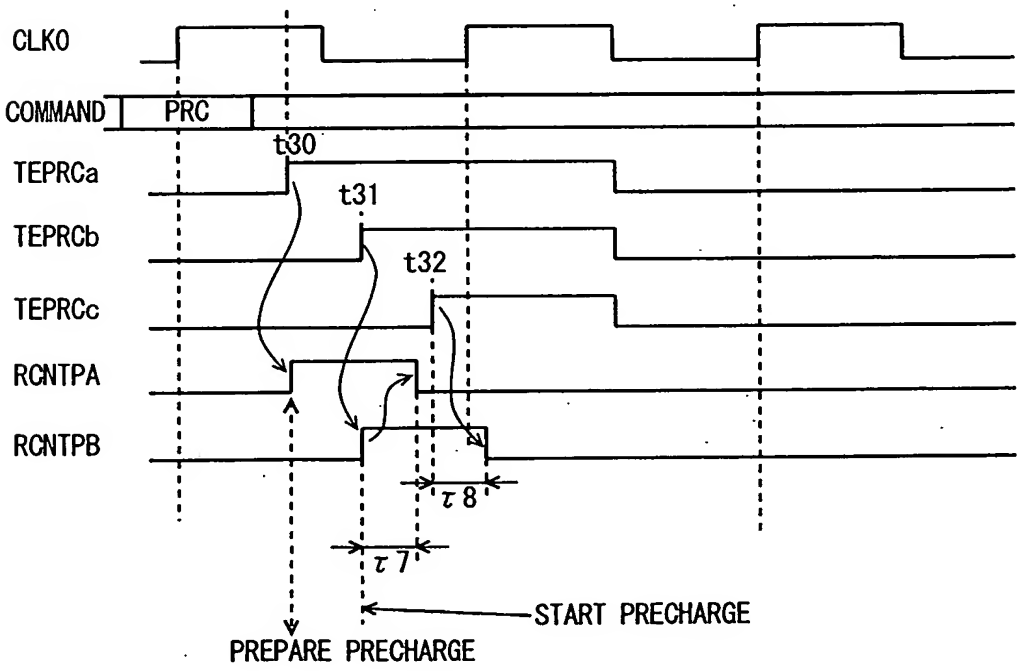

CLKO
COMMAND
PRC
t30
TEPRCa
t31
TEPRCb
t32
TEPRCc
RCNTPA
RCNTPB
τ 8
τ 7
START PRECHARGE
PREPARE PRECHARGE

FIG.77

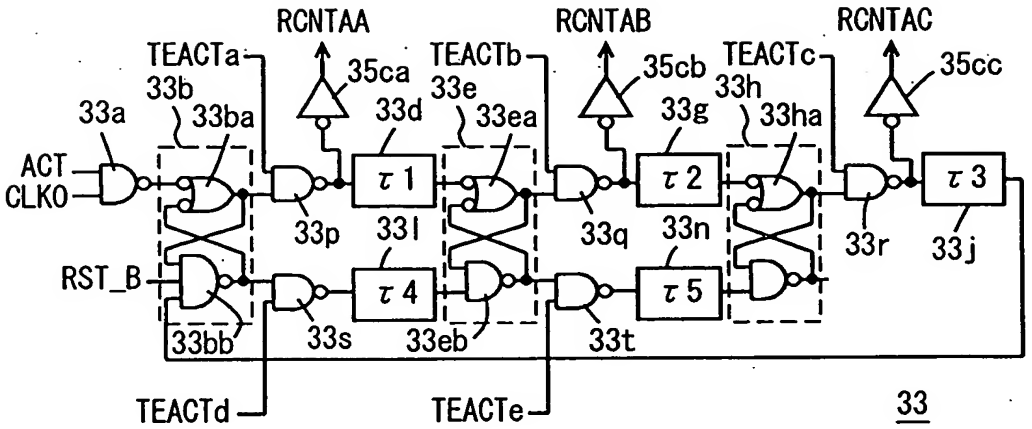

RCNTAA
RCNTAB
RCNTAC
TEACTa
TEACTb
TEACTc
33b
33e
33h
35ca
35cb
35cc
33a
33ba
33d
33ea
33g
33ha
ACT
CLKO
τ1
τ2
τ3
33p
33l
33q
33n
33r
33j
RST_B
τ4
τ5
33bb
33s
33eb
33t
TEACTd
TEACTe
33

FIG.78

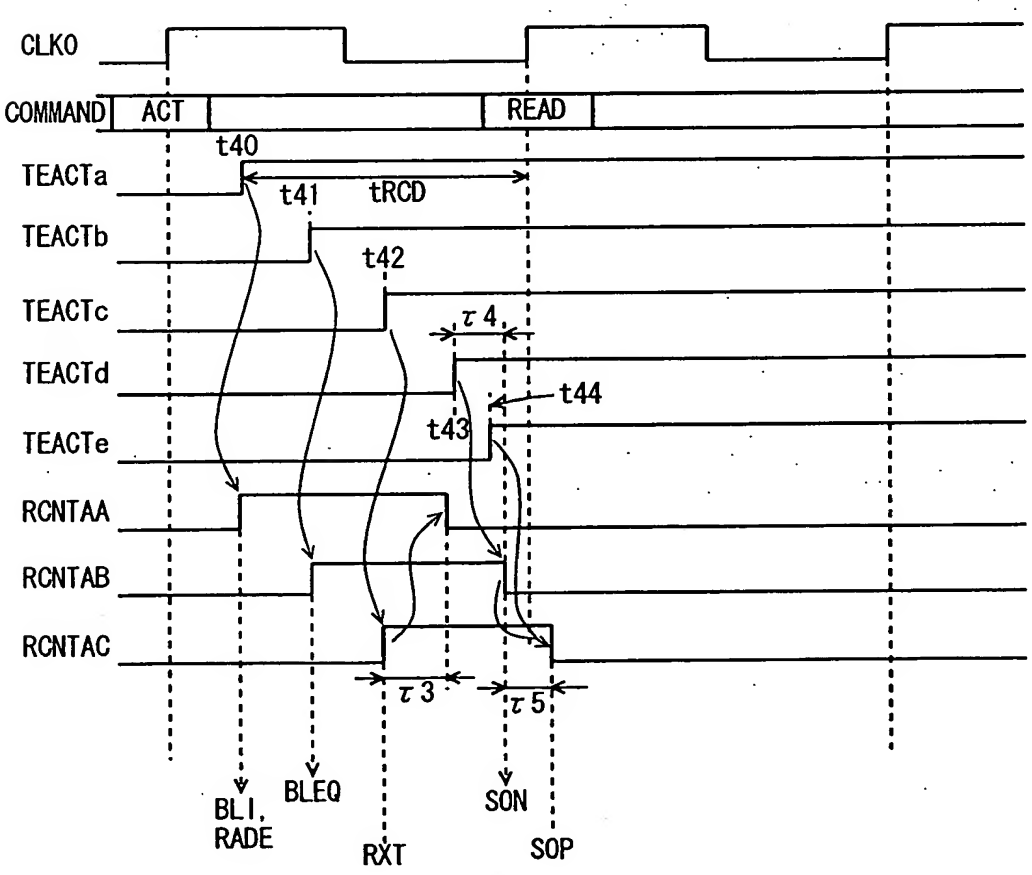

CLKO
COMMAND
ACT
READ
t40
TEACTa
t41
tRCD
TEACTb
t42
TEACTc
τ4
TEACTd
t44
t43
TEACTe
RCNTAA
RCNTAB
RCNTAC
τ3
τ5
BLI,
RADE
BLEQ
RXT
SON
SOP

FIG.79 PRIOR ART

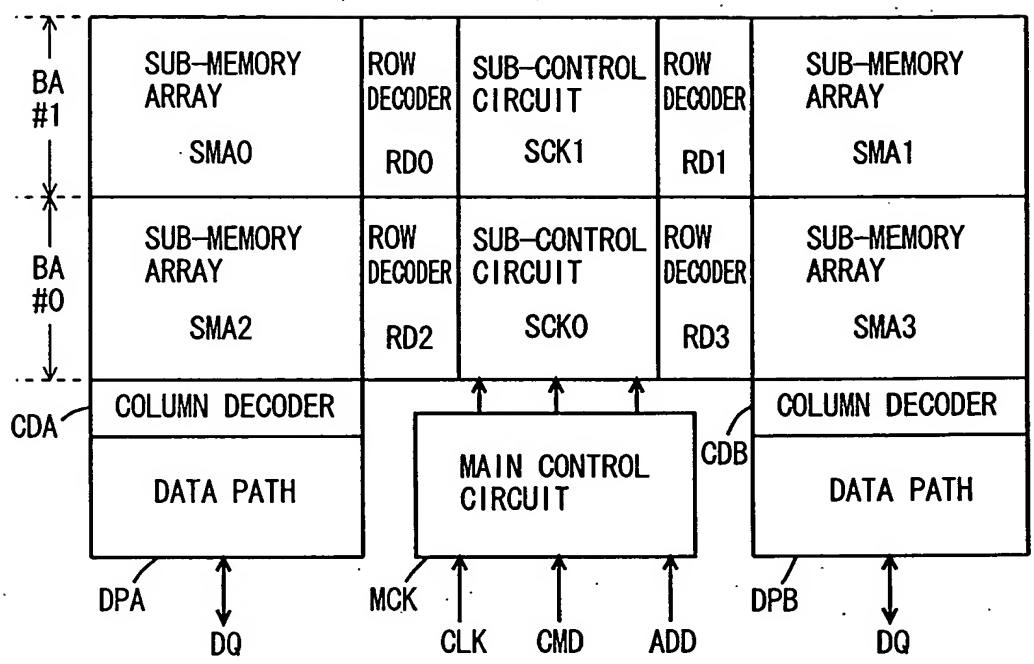



FIG.80 PRIOR ART

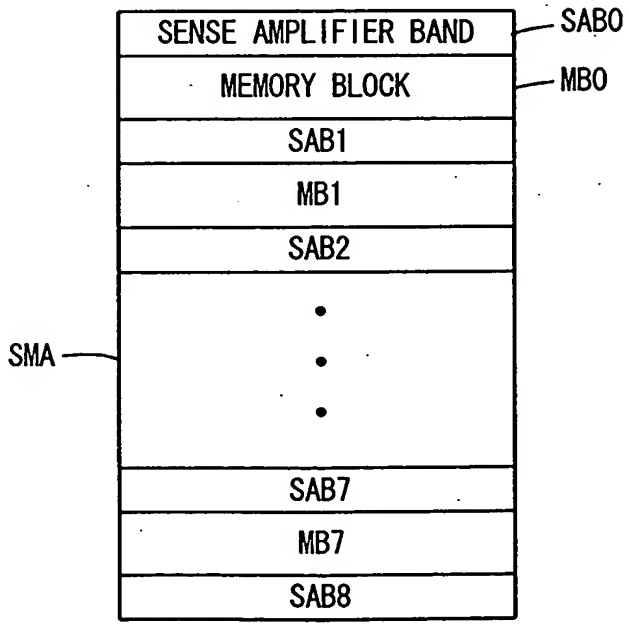


FIG.81 PRIOR ART

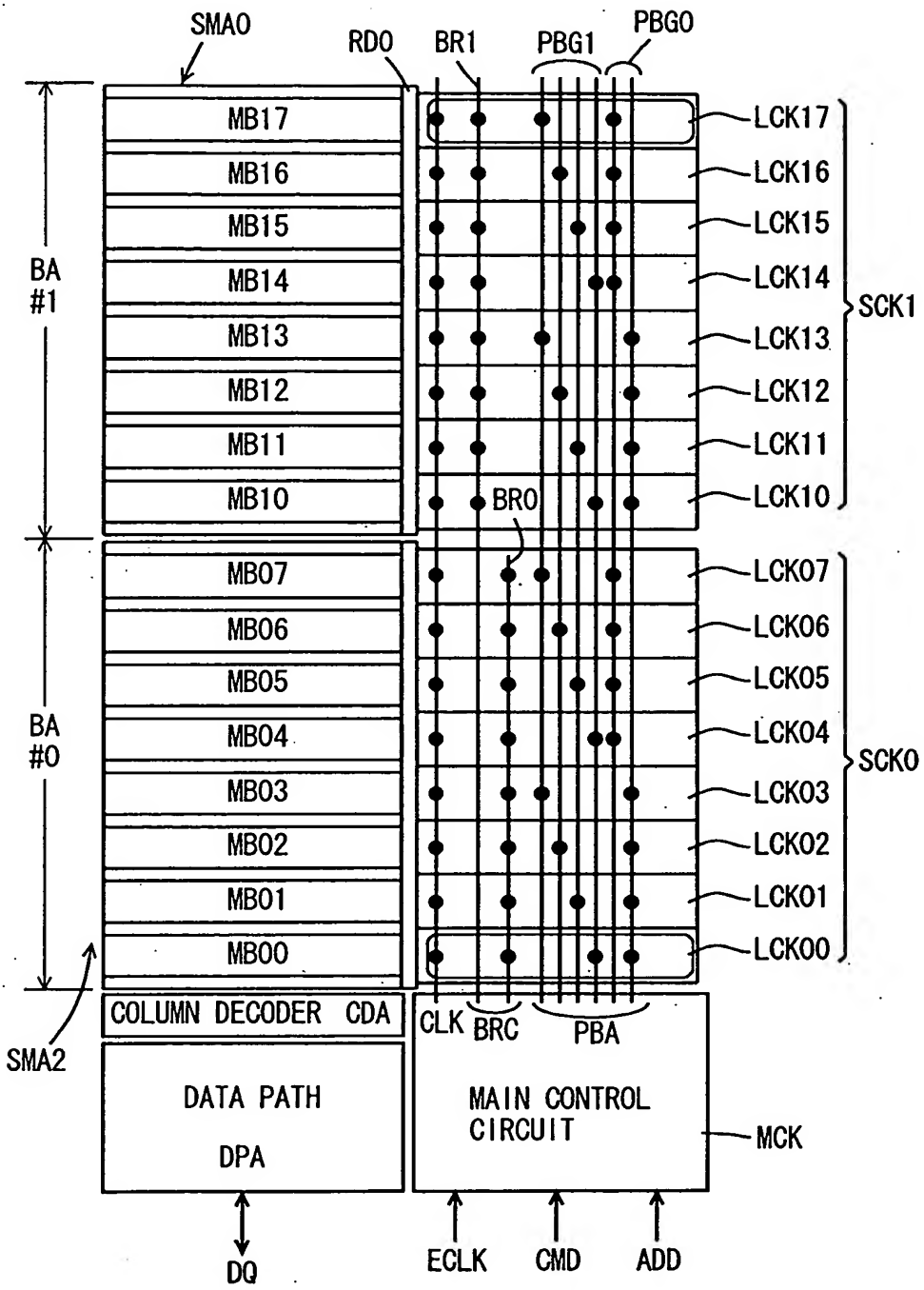


FIG.82 PRIOR ART

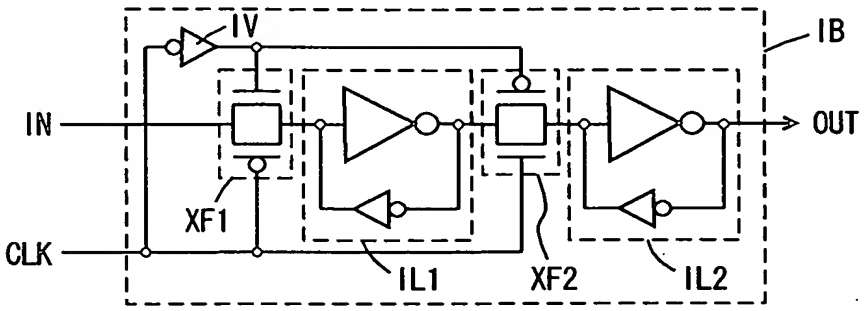



FIG.83 PRIOR ART

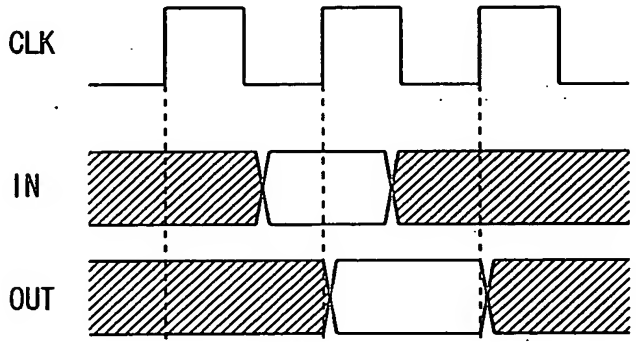



FIG.84 PRIOR ART

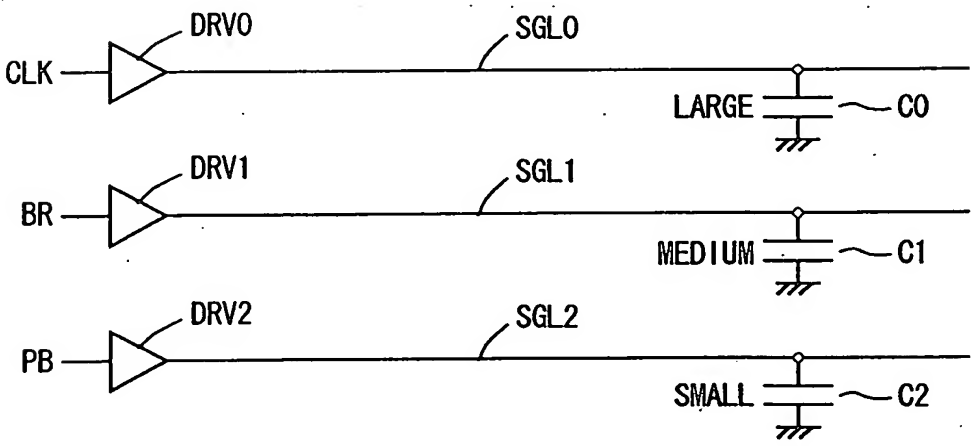


FIG.85 PRIOR ART

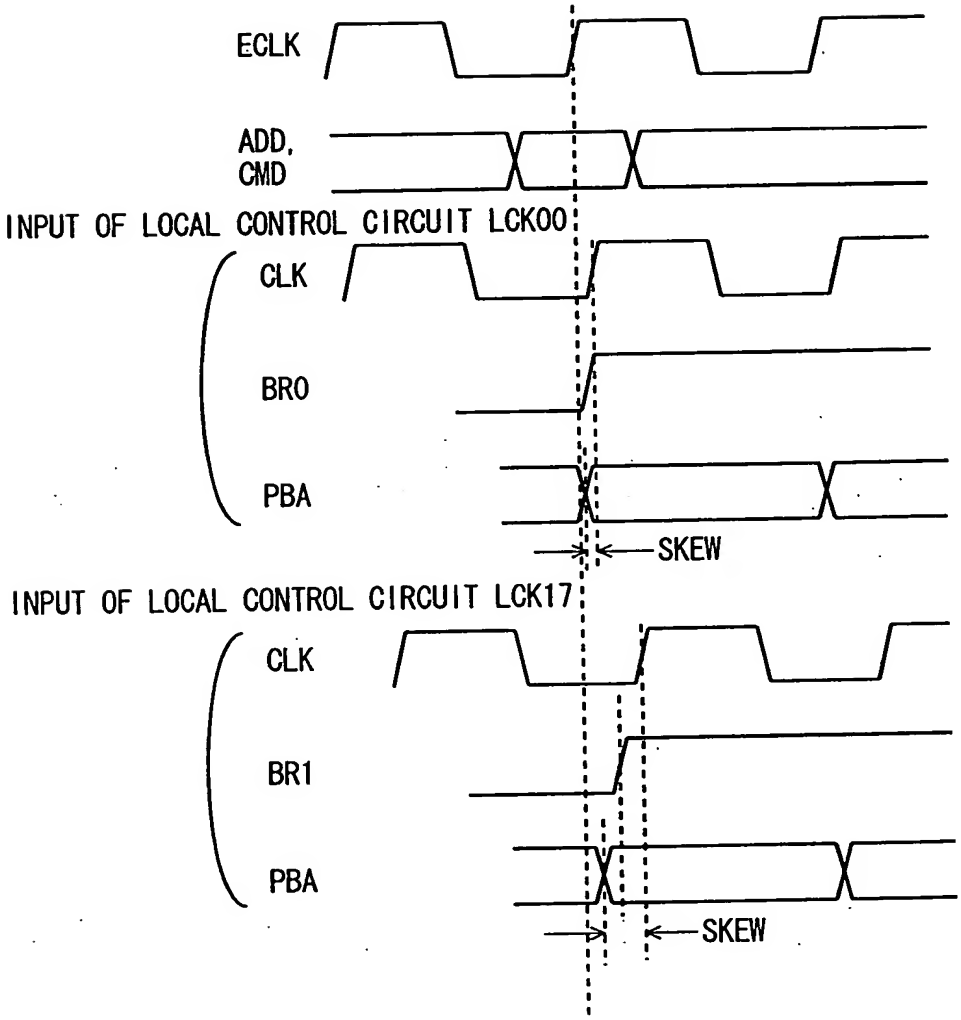


FIG.86 PRIOR ART

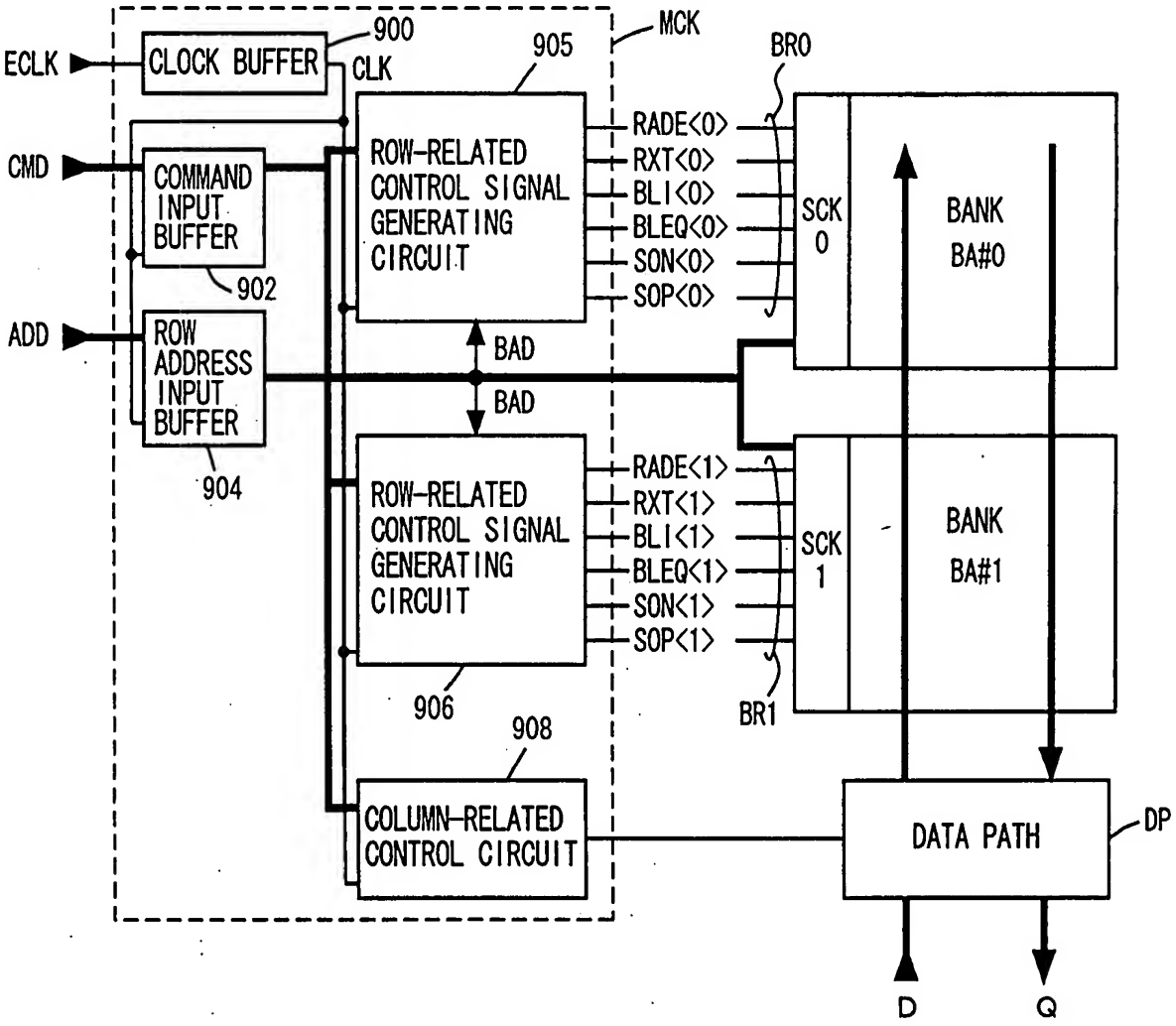


FIG.87 PRIOR ART